AMD and IBM Detail Early Results Using Immersion and Ultra Low-K in 45nm Chips

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At the International Electron Device Meeting today, IBM and AMD presented papers describing the use of immersion lithography, ultra-low-K interconnect dielectrics, and multiple enhanced transistor strain techniques for application to the 45nm microprocessor process generation. AMD and IBM expect the first 45nm products using immersion lithography and ultra-low-K interconnect dielectrics to be available in mid-2008.

“As the first microprocessor manufacturers to announce the use of immersion lithography and ultra-low-K interconnect dielectrics for the 45nm technology generation, AMD and IBM continue to blaze a trail of innovation in microprocessor process technology,” said Nick Kepler, vice president of logic technology development at AMD. “Immersion lithography will allow us to deliver enhanced microprocessor design definition and manufacturing consistency, further increasing our ability to deliver industry-leading, highly sophisticated products to our customers. Ultra-low-K interconnect dielectrics will further extend our industry-leading microprocessor performance-per-watt ratio for the benefit of all of our customers. This announcement is another proof of IBM and AMD’s successful research and development collaboration.”

Current process technology uses conventional lithography, which has significant limitations in defining microprocessor designs beyond the 65nm process technology generation. Immersion lithography uses a transparent liquid to fill the space between the projection lens of the step-and-repeat lithography system and the wafer that contains hundreds of microprocessors. This significant advance in lithography provides increased depth of focus and improved image fidelity that can improve chip-level performance and manufacturing efficiency. This immersion technique will give AMD and IBM manufacturing advantages over competitors that are not able to develop a production-class immersion lithography process for the introduction of 45nm microprocessors. For example, the performance of an SRAM cell shows improvements of approximately 15 per cent due to this enhanced process capability, without resorting to more costly double-exposure techniques.

In addition, the use of porous, ultra-low-K dielectrics to reduce interconnect capacitance and wiring delay is a critical step in further improving microprocessor performance as well as lowering power dissipation. This advance is enabled through the development of an industry-leading ultra-low-K process integration that reduces the dielectric constant of the interconnect dielectric while maintaining the mechanical strength. The addition of ultra-low-K interconnect provides a 15 per cent reduction in wiring-related delay as compared to conventional low-K dielectrics.

“The introduction of immersion lithography and ultra-low-K interconnect dielectrics at 45nm is an early example of the successful transfer of technology from our ground-breaking research work at the Albany Nanotech Center to IBM’s state-of-the-art 300mm manufacturing and development line at East Fishkill, New York, as well as AMD’s state-of-the-art 300mm manufacturing line in Dresden, Germany,” said Gary Patton, vice president, technology development at IBM’s Semiconductor Research and Development Center. “The successful integration of leadership technologies with AMD and our partners demonstrates the strength of our collaborative innovation model.”

The continued enhancement of AMD and IBM’s transistor strain techniques has enabled the continued scaling of transistor performance while overcoming industry-wide, geometry-related scaling issues associated with migrating to 45nm process technologies. In spite of the increased packing density of the 45nm generation transistors, IBM and AMD have demonstrated an 80 per cent increase in p-channel transistor drive current and a 24 per cent increase in n-channel transistor drive current compared to unstrained transistors. This achievement results in the highest CMOS performance reported to date in a 45nm process technology.

IBM and AMD have been collaborating on the development of next-generation semiconductor manufacturing technologies since January 2003. In November 2005, the two companies announced an extension of their joint development efforts until 2011 covering 32nm and 22nm process technology generations.

Source: AMD