UMC Produces Working 45-nanometer ICs

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UMC, a leading global semiconductor foundry, today announced that it has successfully produced functional 45-nanometer SRAM chips that feature an impressive bit cell size of less than 0.25um2. The ICs, produced using UMC's independently developed logic process, used sophisticated immersion lithography for its 12 critical layers and incorporated the latest technology advancements such as ultra shallow junction, mobility enhancement techniques, and ultra low-k dielectrics (k=2.5).

Immersion lithography is a resolution enhancement technique that interposes a liquid medium between the scanner optics and the wafer surface, replacing the traditional air gap. The optical resolution is enhanced since the immersion fluid, which has a higher refractive index than air, allows using lenses with a higher numerical aperture. The result is more accurate patterns imprinted on the silicon wafer.

Dr. Shih-Wei Sun, executive vice president of UMC's Central R&D Division and Fab 12A, commented, "This latest achievement demonstrates that UMC's commitment to process technology leadership is stronger than ever. The 45nm node is a challenging technology generation that simultaneously introduces new materials and process modules. We are excited to be among the first companies in the world to produce working 45nm silicon, and are encouraged by the successful results realized for the initial 45nm wafer lots. UMC will continue to build on its 45nm momentum to enhance yields and prepare the technology for adoption by our foundry customers."

The 45nm SRAM memory bit-cell and macro circuit require good minimum supply voltage capability, an area that UMC has been paying special attention to since the early stages of 45nm process development. Good minimum supply voltage capability is an important aspect for 45nm due to the demanding power saving requirements of today's advanced portable electronics. In addition, by using optional circuits built into the test vehicle, the minimum supply voltage level can be further improved to achieve excellent power behavior.

Producing working SRAM is a key first-step in demonstrating technology performance and process reliability prior to engaging customers for the manufacturing of their 45nm products. UMC's 45nm process features a 30 percent design rule shrink, 50 percent 6-transistor SRAM cell size shrink, and a 30 percent device performance gain over the 65nm technology node, which is in production at UMC for several customer products. Development for UMC's 45nm process is taking place at the foundry's 300mm Fab 12A, located in Tainan Science Park in southern Taiwan.

Source: UMC

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