

# How can we make nanoscale capacitors even smaller?

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Researchers at UC Santa Barbara have discovered what limits our ability to reduce the size of capacitors, often the largest components in integrated circuits, down to the nanoscale. They have answered a 45-year old question: why is the capacitance in thin-film capacitors so much smaller than expected?

Because there is great interest in increased portability in consumer electronics, researchers are continually searching for ways to reduce the size of electronic devices, but capacitors have proved particularly problematic. Researchers have tried to use high-permittivity materials to achieve more capacitance in a smaller area, but nanoscale devices have yielded lower-than-expected capacitance values. These low values have limited the performance of thin-film capacitors and prevented further device miniaturization.

Nicola Spaldin, a professor in the Materials Department of the College of Engineering, and her collaborator, post-doctoral researcher Massimiliano Stengel, used quantum mechanical calculations to prove that a so-called "dielectric dead layer" at the metal-insulator interface is responsible for the observed capacitance reduction.

Spaldin and Stengel explain, in the October 12 issue of *Nature*, that the fundamental quantum mechanical properties of the interfaces are the root cause of the problem, and show that metals with good screening properties can be used to improve the properties. "Our results provide practical guidelines for minimizing the deleterious effects of the

dielectric dead layer in nanoscale devices," they say.

Source: UC Santa Barbara

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