IMEC demonstrates multimedia decoding on reconfigurable processor with record power efficiency

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IMEC developed a reconfigurable processor for video decoding achieving power efficiencies 6 to 12 times higher than state-of-the-art C-programmed processors. The processor was derived from IMEC's C-programmable ADRES (Architecture for Dynamically Reconfigurable Embedded Systems) using its corresponding compiler. It proves that ADRES and its compiler are very well suited for time efficient integration in future low-power portable wireless multimedia devices.

The processor was developed to support multi-format MPEG-2, MPEG-4 and H.264/AVC video decoding at resolutions ranging from QVGA up to D1. Its functionality is demonstrated for 30 frames per second H.264/AVC video decoding at CIF resolution by means of an FPGA (field-programmable gate array) implementation. To decode CIF resolution video in real time, the multimedia ADRES processor is only used for 1/6 of its total capacity (50MHz), resulting in a simulated power consumption of around 17mW for an ASIC implementation. The result proves the high performance efficiency of ADRES requiring only one single ADRES processor for handling 30fps H264/AVC video decoding at for example VGA (50mW, 150MHz) and D1 (68mW, 205MHz) resolutions.

ADRES, developed in the context of IMEC's multi-mode multimedia (M4) program, is a new type of power-efficient, flexible computer architecture template designed to cope with the challenges presented by

multimedia and wireless baseband processing for future mobile terminals. For each application domain, a specific ADRES instance is generated from a generic architecture template and is customized to optimally support the required computation at minimal power. One of its unique points is that it combines state-of-the-art power efficiency with programmability in a high level programming language (C) for a complete application, which is of primary importance for short time-to-market.

Current research focuses on the application of the ADRES processor in a multi-processor platform for multi-format video decoding and encoding up to HDTV resolution H.264/AVC.

"With this demonstrator, we achieved a very important milestone in our multi-mode multimedia program. It shows that the ADRES architectural template as well as the corresponding compiler are sufficiently stable and operational for transfer to support industrial product development;" said Rudy Lauwereins, Vice President Design Technology for Integrated Information and Communication Technology at IMEC.

This result was achieved in collaboration with IMEC's M4 partners Samsung and Freescale and with the support of Barco Silex, Barco's center of competence for micro-electronic design.

Source: IMEC