IMEC demonstrates feasibility of double patterning immersion litho for 32nm node

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IMEC showed in collaboration with ASML the potential of double patterning 193nm immersion lithography at 1.2NA for 32nm node Flash and logic.

These results prove that double patterning might be an intermediate solution before extreme ultraviolet (EUV) lithography and very high NA (beyond water) 193nm immersion lithography will be ready for production. Meanwhile, installation of both ASML's XT:1700i immersion scanner and EUV alpha demo tool (ADT) runs at full speed in IMEC's 300mm clean room.

The very promising double patterning results were obtained by splitting gate levels of 32nm half pitch Flash cells as well as logic cells in two complementary designs. The splitting was done automatically using software from EDA partners in IMEC's lithography program. After splitting, both designs received optical proximity corrections (OPC) and a classical lithography approach "litho-etch-litho-etch" was performed. Exposures of both lithography steps have been carried out on a XT:1700i at ASML.

These results prove that the XT:1700i 193nm immersion tool, which has a maximum NA of 1.2, can be extended beyond the 45nm node. Since both hyper NA 193nm immersion lithography using high-index liquids and EUV still require a lot of research, IC manufacturers welcome double patterning as a solution to continue their research on material integration for the 32nm node.

During the last week of September, the ASML XT:1700i was delivered at IMEC and is currently being installed around the clock. The XT:1700i system is expected to pass the site acceptance tests by the end of the month and will be the workhorse for the double patterning work at IMEC. Future research on double patterning will focus on improving the overlay to make it a reproducible process.

Although quite some development is required to bring EUV production ready, EUV lithography is the preferred option for many companies for the 32nm half pitch node due to its extendibility to 22nm and beyond. Since the arrival of ASML's EUV advanced demo tool (ADT) mid August, significant progress has been made in the installation. Integration of the system (including the projection optics box of Carl Zeiss and the EUV light source of Philips Extreme UV) has started and will continue over the next months. During and after this period, ASML will work on the verification and qualification of the various sub-modules in the tool. Also the TEL Clean Track Act12, connected to the EUV tool, is under installation.

"We are very pleased with the progress that we've made the last months both on immersion and EUV lithography;" said Luc Van den hove, Vice President Silicon Process and Device Technology at IMEC. "We are convinced that our advanced lithography program will offer our partners early lithography solutions to continue CMOS scaling beyond 32nm."

Source: IMEC