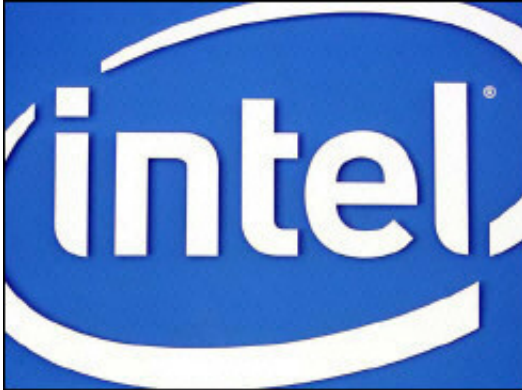# Intel Develops Tera-Scale Research Chips

September 26 2006

Intel Corporation today described the significant technical challenges that need to be addressed if computing, from personal devices to giant data centers, is to keep up with increasing demand by consumers and businesses for Internet-based software, services and media-rich experiences.

In a speech today at the Intel Developer Forum, Intel Senior Fellow and Chief Technology Officer Justin Rattner said that during the next decade online software services, hosted by mega data centers with more than a million servers, will allow people to access personal data, media and applications from any high-performance device to play photo-realistic games, share real-time video and do multimedia data mining. This new usage model will challenge the industry to deliver the one trillion floating-point operations-per-second (teraFLOPs) of performance and terabytes

of bandwidth.

"The rise of mega data centers and the need for high-performance personal devices will require the industry to innovate at every level, from many-core processors to higher-speed communications between systems, while delivering better security and energy efficiency," said Rattner. "Solving these challenges will bring benefits to all computing devices while creating new markets and opportunities for developers and systems designers."

Tera-Scale Research Prototype Chips

Rattner outlined the importance of three major silicon breakthroughs. He started by revealing the first details of Intel's tera-scale research prototype silicon, the world's first programmable TeraFLOP processor. Containing 80 simple cores and operating at 3.1 GHz, the goal of this experimental chip is to test interconnect strategies for rapidly moving terabytes of data from core to core and between cores and memory.

"When combined with our recent breakthroughs in silicon photonics, these experimental chips address the three major requirements for tera-scale computing – teraOPS of performance, terabytes-per-second of memory bandwidth, and terabits-per-second of I/O capacity," said Rattner. "While any commercial application of these technologies is years away, it is an exciting first step in bringing tera-scale performance to PCs and servers."

Unlike existing chip designs where hundreds of millions of transistors are uniquely arranged, this chip's design consists of 80 tiles laid out in an 8x10 block array. Each tile includes a small core, or compute element, with a simple instruction set for processing floating-point data, but is not Intel Architecture compatible. The tile also includes a router connecting the core to an on-chip network that links all the cores to each other and

gives them access to memory.

The second major innovation is a 20 megabyte SRAM memory chip that is stacked on and bonded to the processor die. Stacking the die makes possible thousands of interconnects and provides more than a terabyte-per-second of bandwidth between memory and the cores.

Rattner demonstrated a third major innovation, the recently announced Hybrid Silicon Laser chip developed in collaboration with researchers at University of California, Santa Barbara. With this breakthrough, dozens or maybe hundreds of Hybrid Silicon Lasers could be integrated with other silicon photonic components onto a single silicon chip. This could lead to a terabit-per-second optical link capable of speeding terabytes of data between chips inside computers, between PCs, and between servers inside data centers.

More information on these developments and tera-scale computing research can be found at www.intel.com/go/terascale .

Source: Intel