

## IBM, Chartered, Infineon And Samsung Announce Process And Design Readiness For Silicon Circuits On 45nm Low-Power Techno

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IBM, Chartered Semiconductor Manufacturing, Infineon Technologies, and Samsung Electronics Co., Ltd. today announced first siliconfunctional circuits and the availability of design kits based on their collaboration for 45nm low-power process technology.

The early characterization of key design elements in silicon, coupled with the availability of early design kits, provide designers with a significant head start in moving to the latest process from the industry-leading CMOS technology research and development alliance. The early design kits are developed through a collaborative effort by all four companies and are immediately available for select customers.

The first working circuits in 45nm technology, targeted at next-generation communication systems, were proven in silicon using the process technology jointly developed by the alliance partners and were produced at the IBM 300-millimeter (mm) fabrication line in East Fishkill, NY, where the joint development team is based. Among the successfully verified blocks are standard library cells and I/O elements provided by Infineon, as well as embedded memory developed by the alliance. Infineon has included special circuitry on the first 300mm wafers to debug the complex process and to gain experience in product architecture interactions.

"This result is another significant milestone in our successful strategy to



develop optimized product solutions using the most advanced technology platforms as early as possible," stated Hermann Eul, member of the board of Infineon Technologies and president of its Communication Solutions business group. "The first structures in 45nm represent our most cutting-edge technology, bringing together high-performance capabilities and low-power consumption. This solution is clearly well-suited to address the needs of next-generation mobile applications."

The development of the design kits incorporates design expertise from all four companies in order to facilitate earlier transition to the new process by chip customer designers, as well as to continue to drive single-design, multi-fab manufacturing capability for maximum design leverage and to bring about ultimate consumer benefit. The 45nm low-power process is expected to be installed and fully qualified at Chartered, IBM and Samsung 300mm fabs by the end of 2007.

"The speed, innovation and completeness with which this first 45nm offering has been developed and made available to customers demonstrates the growing customer value and strength of the partnership between these four companies. Our early hardware results indicate that the 45nm node device performance is at least 30 percent greater than that of the 65nm node, and that product developers can design to this process with confidence," said Lisa Su, vice president of semiconductor research and development at IBM and the head of the joint development alliance. "By leveraging the significant R&D and IP resources available worldwide across this alliance of industry leaders, we are able to bring manufacturing technology and design readiness to the market much sooner and effectively for customers than working individually. And, the additional benefit to customers is the flexibility in accessing the technology thanks to the GDSII compatibility across multiple manufacturing facilities."

"The unique cooperation among IBM, Chartered, Infineon and Samsung



reduces the inherent risks in adoption of advanced process technology," said Ho-Kyu Kang, vice president of the advanced technology development team at Samsung Electronics' System LSI Business. "Our customers leverage the combined strengths of our system level, product design, and manufacturing expertise in the development of leadership design kits and process technology."

Source: Samsung Electronics

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