

Panasonic Develops the World's First GaN Vertical Transistor

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Panasonic today announced the development of a Gallium Nitride (GaN) transistor with vertical structure which dramatically reduces the chip size comparing with the conventional planar structure. This is the world's first demonstration of GaN vertical transistor applicable to high power switching devices.

The GaN vertical transistor features a submicron channel fabricated using novel self-aligned process. This device configuration effectively reduces the device area down to one-eighth of the conventional planar device. The submicron channel with the width of 0.3 μ m serves good pinch-off characteristics that are strongly required for power switching



devices.

Another feature of the vertical transistor is low on-state resistance by the reduction of contact resistance at the top electrode. Panasonic's proprietary epitaxial growth technology of InAlGaN quaternary alloy enables low contact resistance by using it as a contact layer. The InAlGaN effectively reduces the barrier height from the electrode resulting in one-third lower contact resistance than the conventional one.

In addition, the GaN vertical transistor successfully suppresses current collapse that has been commonly observed in GaN-based transistors. The current collapse is the phenomena in which drain current is reduced at high voltage operation mainly by the charges trapped at the surface. The vertical transistor has smaller surface area so that the effect of the surface trap is fully suppressed.

Applications for seventeen domestic and ten international patents have been filed. These research and development results have been presented at Device Research Conference 2006, held at Pennsylvania State University, Pennsylvania, U.S. from June 26 to 28, 2006.

Source: Matsushita Electric

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