Intel Researchers Improve Tri-Gate Transistor

June 13 2006

Intel Corporation researchers today disclosed they have developed new technology designed to enable next era in energy-efficient performance. Intel's research and development involving new types of transistors has resulted in further development of a tri-gate (3-D) transistor for high-volume manufacturing. Since these transistors greatly improve performance and energy efficiency Intel expects tri-gate technology could become the basic building block for future microprocessors sometime beyond the 45nm process technology node.

Planar (or flat) transistors were conceived in the late 1950s and have been the basic building block of chips since the dawn of the semiconductor industry. As semiconductor technology moves deeper into the realm of nanotechnology (dimensions smaller than 100nm), where some transistor features may consist of only a few layers of

atoms, what was previously thought of as "flat" is now being designed in three dimensions for improved performance and power characteristics. Intel, leading the industry in producing high volumes of ever smaller chip geometries, has created a way to use these three-dimensional, or tri-gate, transistors in concert with other key semiconductor technologies to enable a new era of energy-efficient performance.

Tri-gate transistors are likely to play a critical role in Intel's future energy efficient performance capabilities because they offer considerably lower leakage and consume much less power than today's planar transistors. Compared to today's 65nm transistors, integrated tri-gate transistors can offer a 45 percent increase in drive current (switching speed) or 50 times reduction in off-current, and 35 percent reduction in transistor switching power. Increased performance and reduced energy consumption improve the experience for users of PCs and other devices using Intel platforms.

"These results demonstrate that Intel is taking a leadership approach to new advancements," said Mike Mayberry, Intel vice president and director of component research. "Intel has successfully integrated three key elements -- tri-gate transistor geometry, high-k gate dielectrics, and strained silicon technology -- to once again produce record transistor capabilities. These results give us high confidence that we can continue Moore's Law scaling well into the next decade."

Intel technologists will present a technical paper on this research on June 13 at the 2006 Symposium on VLSI Technology in Honolulu.

Source: Intel