Samsung Develops 3D Memory Package that Greatly Improves Performance Using Less Space

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Samsung Electronics announced today that it has developed a small-footprint, wafer-level processed stack package (WSP) of high density memory chips using 'through silicon via' (TSV) interconnection technology. WSP actually reduces the physical size of a stacked set of semiconductor chips, while greatly improving overall performance. Widely seen as the next generation in package technologies, WSP can be applied to all types of hybrid packages, including memory and processors, to deliver higher speed and higher density with minimum use of chip space.

Using this technology, mobile device and consumer electronics manufacturers will gain better electrical performance, well suited for slimmer, high-performance handset designs that provide longer battery time.

Samsung' industry-first WSP is a 16Gbit memory solution that stacks eight 2Gb NAND chips. The WSP generates a much smaller multi-chip package (MCP), which is the current mainstream solution for designing miniaturized, high-capacity memory devices. Samsung's eight-chip WSP prototype sample, which vertically stacks eight 50μ(micrometers), 2Gb NAND flash die, is 0.56 millimeters in height.

The chips in today's MCPs are connected by wire bonding, which requires vertical gaps between dies that are tens of microns wide and

horizontal spaces on the package board that are hundreds of microns wide to accommodate the wire connections. By contrast, WSP forms micron-sized holes that penetrate through the silicon vertically to connect circuits directly, eliminating the need for gaps of extra space and wires protruding beyond the sides of the die. Due to these advantages, WSP has a 15-percent smaller footprint and is 30 percent thinner than an equivalent wire-bonded MCP solution.

Another distinct advantage of Samsung's WSP technology is that it introduces a much simplified process for the TSV. Instead of using a conventional dry etching method, a tiny laser drills the TSV holes. This reduces production cost significantly as it eliminates the typical photolithography-related processes required for mask-layer patterning and also shortens the dry-etching process needed to penetrate through a multi-layer structure.

Also, WSP reduces the length of the interconnections, resulting in an approximately 30-percent increase in performance from reduced electrical resistance. This makes it a more attractive solution for applications requiring lower power consumption, higher performance and higher density, such as today's slimmer handset designs.

Initially, Samsung will apply its WSP technology to the production of NAND-based memory cards for mobile applications and other consumer electronics in early 2007. Later, the company will extend the packaging technique to high-performance system-in-package (SiP) solutions, and high-capacity DRAM stack packages including DRAM modules used in server designs that require fast data processing.

Source: Samsung Electronics