

New concept for bendable packaged ultra-thin chips presented

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IMEC and its associated laboratory INTEC of the University of Ghent jointly developed a new process flow for ultra-thin chip packages resulting in bendable packaged chips of only 50 μ m thickness. The technology enables embedding packaged chips empowering smart, highly-integrated, flexible electronic systems for a wide variety of applications.

The process has been demonstrated with silicon chips thinned down to 20-30 μ m. Thanks to the very low thickness of the chip, polyimide layers and metal, a total thickness down to 50 μ m is achieved making the whole package bendable. The ultra-thin chip package can provide an interposer enabling testing of the chip before embedding. It offers a contact fan out with more relaxed pitches.

Thanks to its flexibility, the technology enables embedding of packaged chips in flexible boards empowering smart, highly-integrated, flexible electronic systems for a wide variety of applications such as smart textile and flexible displays. The process flow has been developed within the EU funded FP6 Integrated Project, SHIFT (Smart high-integration of flex technologies).

The base substrate is a 20 μ m-thick polyimide layer spin-coated on a rigid glass carrier. For the fixation and the placement of the chips on the polyimide layer a bicyclobutane of less than 5 μ m is used as adhesive. Bicyclobutane is resistant to the high curing temperature of the top polyimide since its solvents evaporate during a pre-curing.

By placing the chips properly, either in vacuum or with a dispensed bicyclobutane, void-free bonds can be obtained.

Current research focuses on the optimization of the chip placement on dispensed (pre-cured) bicyclobutane and on avoiding voids by controlling the dispensed quantity. In this way, no vacuum environment will be required.

After the cure of the bicyclobutane at 350°C, the chip is fixed on the polyimide layer. A covering polyimide layer is spin-coated on the fixed die with a thickness of 20µm. For contacting to the chip, contact openings to the bumps of the chips are laser drilled. By using a shaped laser beam, via diameters with a top diameter down to 20µm can be realized.

A top metal layer of 1µm TiW/Cu is sputtered and photolithographically patterned, metallizing the contacts to the chip and providing a fan out to the contacts of the chips. Finally, the whole package is released from the rigid carrier.

Source: IMEC

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