GA Tech develops ultra-efficient embedded architectures based on probabilistic technology

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Researchers at the Georgia Institute of Technology announce energy savings by a factor of more than 500 in simulations with their ultra energy efficient embedded architecture based on Probabilistic CMOS (PCMOS).

The research team's PCMOS devices take advantage of noise, currently fabricated at the quarter-micron (0.25 micron) level, and uses probability to extract great energy savings. The findings will be presented at the Design, Automation and Test In Europe (DATE) Conference, the leading peer-reviewed European electronic systems design meeting, on March 9 in Munich, Germany.

The research team led by Dr. Krishna Palem, a joint professor in the Georgia Tech College of Computing and the School of Electrical and Computer Engineering and founding director of the Center for Research in Embedded Systems & Technology, has confirmed that architectural and application gains to be reported at DATE are as high as a factor of 560 when compared to comparable CMOS based architectures. As traditional CMOS semiconductor technology approaches the nanoscale, coping with noise and energy savings are increasingly important.

PCMOS harnesses the inherent instability of noise and uses it as a resource to achieve energy efficient architectures. In the architectures, noise induces distortion in the application. However, given the human

ability to average this routinely such as in voice when using cell phones, or in images when they are streamed to hand held devices, the user does not often notice the distortion as significant and is willing to pay the price for significant energy savings. A demonstration showing this effect in the context of video decompression used in modern DVD images is available for viewing at Source: http://www.crest.gatech.edu/palempbitscurrent/demo.html.

"Probabilistic architectures extend PCMOS to computing substrates beyond devices," says Palem. "By mixing chip measurements and simulations, gains have been shown using this technology for such applications as Hyper-encryption as applied to computer security, and through cognitive applications such as speech recognition and pattern recognition as well as image decompression. The gains ranged from a factor of 10 to a factor of more than 500 over conventional architectural approaches."

Beyond such architectural objectives, when applications need random sources, historically pseudo-random numbers generators were used. The Georgia Tech research team used the National Institute of Standards and Technology (NIST) recommended tests to quantify and measure the quality of randomness of PCMOS within this limited context of being viewed as a source of random bits, beyond complete Probabilistic System on Chip (PSoC) architectures. PCMOS outperformed CMOS in the quality of random sequences generated.

The research team will work on developing PSoC architectures to be fabricated using devices of 180 nanometers, for specific applications with an embedded flavor such as video, and audio signal processing (DSP). Palem estimates this will take nine months to validate.

Source: Georgia Institute of Technology