Renesas Develops Massively Parallel Processor Based on Matrix Architecture

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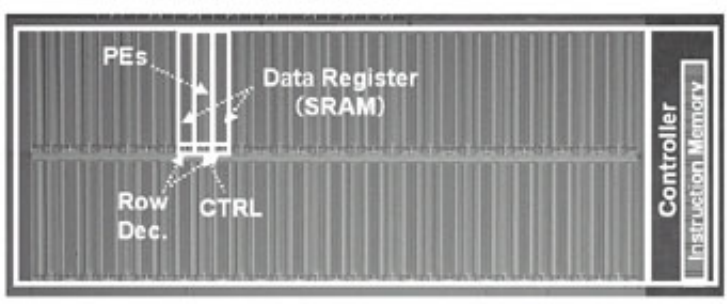

Chip micrograph of Matrix Architecture Processor

Renesas Technology Corp. today announced the development of a massively parallel processor based on a matrix architecture suitable for image and audio multimedia data processing.

This innovatively configured processor is a massively parallel programmable device featuring tight coupling of 2,048 processing elements and 1Mbit SRAM, and has been confirmed to achieve 40 GOPS (giga operations per second) performance at a 200 MHz clock frequency.

Renesas Technology researchers unveiled details at the 2006 IEEE International Solid-State Circuits Conference (ISSCC) being held in San Francisco from February 5.

The image and audio multimedia data processing capability is essential for digital home appliances and other electronics, and involves a combination of complex operations such as fast Fourier transform, convolution, and sum of absolute difference operations. Up to now, processing of these operations has generally used hard-wired logic circuits or a DSP (digital signal processor) specialized for digital signal processing. However, recent dramatic advances in multimedia applications such as the rapid increase in pixel counts in image applications have increased demands for major improvements in multimedia data processing performance. At the same time, there is a growing demand for such processing to be implemented by means of programmable devices in order to simplify support for various multimedia data standards.

One way of improving processing performance is to increase the operating frequency through the use of finer semiconductor processes. However, it will be difficult to continue to gain major improvements in performance while maintaining lower power consumption, and to achieve the required levels of performance with conventional DSP and similar architectures. Meanwhile, a coarse-grained MIMD (multiple instruction multiple data) processor has been announced as an architecture that increases processing performance, but this also has issues with reducing power consumption.

To solve these issues, Renesas Technology has developed a matrix type processor based on a different memory technology from that of a DSP or MIMD type processor.

This new processor is a fine-grained SIMD (single instruction multiple data) type massively parallel programmable device, featuring the following structural characteristics.

1. Basic configuration : 2-bit processing elements (PE) and 512-bit

SRAM assigned as data registers
2. 2,048 PEs and a total of 1 Mbit SRAM, together with tight coupling between Pes .

The key to the increased performance of this processor lies in how efficiently the individual processing elements are operated. Also, the layout and connection of the processing elements and data registers are important factors in achieving reductions in area and power consumption.

A prototype processor using the new technology was implemented in 90 nm CMOS with a core area of 3.1 mm^2, and achieved processing performance of 40 GOPS at a 200 MHz clock frequency and 250 mW power dissipation. These metrics show approximately 70 and 13 times better energy efficiency in terms of unit area ratio and unit power ratio, respectively, compared to a conventional in-house DSP.

Source: Renesas Technology