

Nanotech SRAM for battery devices unveiled

February 9 2006

Researchers have unveiled a SRAM test device for battery-powered devices with the lowest voltage requirements ever produced.

Texas Instruments said the 256-kilobit SRAM (static random access memory) test device is being considered for the next generation of mobile products that will require high performance and low power consumption.

The development of the SRAM device was announced Wednesday at a conference in San Francisco.

The device was created in conjunction with the Massachusetts Institute of Technology using TI's 65-nanometer CMOS (complementary metal oxide semiconductor) process. It boasts a 0.4 volt sub-threshold with twice as less power leakage as current models that operate at 0.6 volts.

"Scaling to such low supply voltages is critical to minimum energy processing and enables Ultra-Dynamic Voltage Scaling," said MIT Professor Anantha Chanrakasan. "The goal of this ultra-low power technology is to reduce energy ... with minimal loss in system performance."

Copyright 2006 by United Press International

Citation: Nanotech SRAM for battery devices unveiled (2006, February 9) retrieved 3 May 2024

from <https://phys.org/news/2006-02-nanotech-sram-battery-devices-unveiled.html>

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.