Europe takes leading role in developing chip design tools for next-generation wireless applications

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Philips Electronics, austriamicrosystems, MAGWEL, IMEC and the universities of Lisbon, Bucharest and Delft today announced that they have joined forces in the 'CHAMELEON-RF' project - a European Union IST (Information Society Technologies) 6th Framework Program project targeted at producing better tools for designing the complex nano-scale silicon chips at the heart of next-generation wireless communication products.

By allowing the RF (Radio Frequency) circuits needed in these products to be efficiently and reliably integrated into low-cost silicon chips, these design tools will help to ensure the timely introduction of ever-more advanced communication products that keep consumers connected wherever they are.

"The objective of the CHAMELEON-RF project is to provide chip designers with the electronic design automation tools they need in order to achieve right-first-time RF designs," says Dr. Wil Schilders, Chairman of the CHAMELEON-RF consortium. "To do that we aim to create computer models that will allow silicon-accurate simulation of complete RF circuit blocks rather than single components."

The group will develop simulation models that accurately predict the behavior of RF silicon integrated circuits at frequencies up to 60 GHz. This very high frequency, which is over ten times the highest radio

frequency currently used in typical consumer products, is considered necessary to enable next-generation, high data-rate wireless connectivity systems. These models will take into account the fundamental physical principles of the electrical current flow in circuits and devices and the electromagnetic fields they generate, as well as the electromagnetic interaction between these fields and the circuit components. They will also take into account the effect of process variations in the semiconductor processes used to fabricate the chips. The results will be built into simulation models that will run within the computational constraints of typical EDA (Electronic Design Automation) workstations, enabling them to be incorporated into commercial EDA tools.

The latest multi-band GSM mobile phones are already capable of processing the radio frequencies required to operate across five different continents. They may even incorporate Bluetooth wireless technology, Wi-Fi connections, GPS (Global Positioning System) and Digital TV receivers. Probable new additions will include UWB (Ultra WideBand) for wireless USB connections and Wi-Max for mobile Internet access. Similar wireless connectivity is also appearing in PDAs, lap-top computers and games consoles. Implementing this multi-mode multi-band wireless connectivity within the size, weight, cost and power consumption limitations of consumer products will require the necessary RF circuits to be integrated into increasingly complex nano-scale silicon chips.

Although it is a common belief that radio waves are transmitted and received only through a radio's antenna, the truth is that each individual component in an RF circuit acts as its own antenna. As such, each component is capable of radiating and absorbing a small amount of RF energy to and from its local environment. In conventional RF circuits made up of discrete components mounted on a printed circuit board, most components are mounted sufficiently far apart for the effects of

this localized RF radiation to be either minimal or easily screened by enclosing critical components in metal cans.

However, when these circuits are shrunk to nanometer proportions on a silicon chip, the components are sufficiently close together for adjacent devices to mutually interfere with one another via leakage of RF energy from one component to another. At present, there are no EDA (Electronic Design Automation) tools that allow chip designers to take these effects, and other effects such as RF noise carried through the chip's silicon substrate, into consideration. As a result, RF chip design has remained a difficult time-consuming and risky operation, with success or failure frequently depending on the skill of individual designers.

Source: IMEC