A 20-year old mystery mechanism influencing DRAM cell retention time fluctuation clarified

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Hitachi, Ltd., in cooperation with Elpida Memory announced today that they have identified that the leakage current fluctuation of the p-n junction*1) is the primary factor influencing the charge retention time fluctuation of DRAM cells. As DRAM power consumption is strongly influenced by the retention time, clarifying the mechanism involved is expected to contribute to opening the way for new low power DRAM technology.

Today, DRAM is used as the main memory in high-end servers and PC's, and through the advancement of low power technology, is widening its application to other products such as digital consumer appliances and mobile terminals. A DRAM cell consists of one transistor and one capacitor. A write operation of a DRAM cell is performed by charging the capacitor via an on-state cell transistor, while the cell transistor is in an off-state during the charge retention period. DRAM cell retention time however is limited by charge leakage from the capacitor through an off-state transistor channel and/or a p-n junction. A periodical re-write operation, called a refresh operation, is therefore necessary in DRAM.

In 1987, in relation to DRAM retention time, it was reported that there was an extremely small probability that a DRAM cell with a retention time that fluctuates between two values might exist*2). Although this

phenomenon has been known for nearly 20 years, the cause has never been explained. DRAM cells need periodic refresh operations, and to prevent retention failure in all memory cells, a large safety margin accommodating for cell variations in memory retention time is set in current production. In the future, however, as DRAM capacity and integration continue to advance, it will become increasingly difficult to maintain a large safety margin, making it more difficult to achieve stable low-power operation. Thus, clarifying the mechanism behind memory retention time fluctuations was considered an essential step in the development of large capacity highly integrated DRAM.

In response to these issues, Hitachi and Elpida focused on the leakage current of cell transistors as the cause of retention time fluctuation, and used test devices to conduct detailed measurements. Below are three main findings:

(1) Cell transistors with a reversible leakage current fluctuating between two values, exist at a ratio of a few transistors per 10,000 transistors.
(2) The leakage current in the DRAM cell consists of a channel leakage of the cell transistor and a p-n junction leakage, however, the reversible fluctuation only occurs in the case of the p-n junction
(3) The p-n junction leak current fluctuation has a large temperature dependence; easily fluctuating at high temperatures, increasing the frequency of fluctuations between the two values.

Usually, point defects in the depletion layer of a p-n junction increase the leakage-current of the p-n junction. Thus the mechanism generating the reversible fluctuation of p-n junction leakage-current between two values is thought to be the result of a point defect having two different energy levels,*3) and alternating between them. From the thermal characteristic measurements of (3), it was possible to calculate the energy required for transition between the two states, which was found to be approximately 1 eV (electron volt). This value is comparable to the

energy reported in the case of DRAM retention time fluctuation. As a result, it became clear that the direct cause of the reversible fluctuations in retention time can be found in the reversible fluctuations of the p-n junction leakage current.

This study has contributed to the fundamental understanding of memory cell retention performance, which will have a large impact on the continuation of large capacity, highly integrated, low power DRAM development.

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Notes:

*1) A p-n junction is a junction of p-type and n-type semiconductors, which is a basic component of semiconductor devices. A main electrical property of the p-n junction is a rectification: current flows through the p-n junction under forward bias condition, while a current does not flow under reverse bias condition. The p-n junction is also part of an MOS transistor. The p-n junction as mentioned here is a part of DRAM cell transistor.
*2) Reported by IBM at IEDM 1987.
*3) Energy levels: A free electron in a semiconductor crystal can takes any kinetic energy depending on its speed, except in the forbidden band. The forbidden band is an energy region created by the periodicity of the atomic configuration of the semiconductor crystal, which the electron cannot take. When a point defect or contamination occurs, this periodicity is broken, and an energy level is created within the forbidden band. This energy level facilitates charge flow through the p-n junction, contributing to p-n junction leakage.

Source: Hitachi Ltd.