Penn-State Philips CMOS transistor model adopted as industry-wide standard for future nanometer chip design

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Philips and the Pennsylvania State University today announced that their jointly developed PSP (Penn State Philips) complementary metal-oxide semiconductor (CMOS) transistor model has been selected by the Compact Model Council (CMC) as the industry-wide standard for future CMOS chip design. Founded in 1996 and comprised of 31 leading semiconductor companies and circuit simulator suppliers, the CMC is the world's foremost authority for the standardization, implementation and use of transistor models.

The PSP model will now become the industry standard for simulating the behavior of future generations of CMOS transistors produced at the 65-nm technology node and beyond. By allowing designers to accurately predict circuit performance before committing their designs to silicon, this new standard will enable the optimal use of CMOS chip technology in real-world applications. In addition, the standard will facilitate the exchange of chip designs between design groups and the outsourcing of chip fabrication to silicon foundries by allowing everyone to communicate using the same transistor modeling language. As a result, the chips produced will perform better, be less expensive and appear earlier on the market.

“As CMOS takes on new roles beyond the production of purely digital chips, it is important that the industry has a single model that accurately predicts transistor performance under all circuit conditions, including RF and analog circuit behavior,” said Dr. Reinout Woltjer, Department Head of the Device Modeling group at Philips Research. “By basing the PSP model on the fundamental physics of transistor operation, it provides extremely accurate results over the entire operating spectrum from DC to well in excess of 50 GHz.”

“The PSP model incorporates a number of recent advances in MOS device physics and was made possible by the innovative but practical solution of several long-standing theoretical problems of compact MOSFET modeling” said Dr. Gennady Gildenblat, Professor of Electrical Engineering at The Pennsylvania State University. “This made it possible to include all relevant physical effects without significantly increasing model complexity – a prerequisite for scalability of the model to ever-smaller device geometries.”

Because it is based on the underlying physics of CMOS transistor operation, the number of parameters needed in the PSP model is significantly less than that required by other models. This not only means

that the PSP model enables faster circuit simulation. It also means that the simulation results obtained are more accurate. In particular, it accurately models gate leakage, noise and quantum-mechanical effects that will become increasingly significant to circuit performance as CMOS processes are scaled to nanometer proportions. To allow rapid integration into EDA tools, the model is supported by SiMKit – a professional grade software environment that allows it to be directly coupled into popular circuit simulators.

Source: Philips