NEC's Breakthrough to Enhance Functionality of Sub-10nm Transistors

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NEC today announced the development of new breakthrough device technology for low-power, high performance system LSI. Based on the ultimate scaling of conventional bulk planar MOSFETs, the new technology is capable of improving on-off ratio, enhancing the functionality of sub-10nm planar bulk transistors.

The new device technology has been enabled by the following advancements:

(1) A new elevated source/drain extension (SDE) structure was created through a silicon selective-epitaxial growth technique, enabling a decrease in junction depth to an effective level and an improvement in turn-off characteristics. The thicker, elevated SDE region realizes a reduction in parasitic resistance and an enhancement in on-current. (The silicon surface for the source/drain doping region was raised with respect to the channel region surface.)

(2) By applying a tunneling epitaxial growth technique to the gap region, created by a selective etching technique, between the silicon-surface and sidewall-material, the thickness of the elevated SDE can be self-aligned and easily controlled. This realizes a reduction in fluctuation of elevation thickness, and improved productivity through ease of manufacturing.

This technology can also be used in realizing low power, high performance system LSI for the 45nm technology generation and beyond in the future.

Although silicon devices have been achieving higher performance and increasingly larger-scaled integration through scaling of dimension size, in recent years it has been predicted that their operation principles are nearing physical limits. NEC decided to test these limits in 2003 when it successfully fabricated planar bulk transistors, whose functionality was proven to be valid for 5nm gate-length devices.

However, at that time, actual operation characteristics, i.e. on-off ratio, were not of a sufficiently high standard owing to the trade-off between the on-current and aggressive scaling, as it is necessary to make source/drain junctions shallower to ensure steady operation with dimensional scaling, and a shallower diffusion layer is more resistive to electrical conduction.

NEC's newly developed device technology has successfully solved this issue. The new technique simultaneously achieves controlled elevation of the source/drain region and a significant improvement in the on-off ratio, even for sub-10nm planar bulk transistors. Its potential was shown by actual test-fabrication carried out by NEC on the world's smallest 6nm transistors. Contrary to hypothesis that the ultimately-scaled transistor structure should have a very specific structure on a specific substrate such as the ultra-thin body SOI (silicon-on-insulator) or double-gate structure, this new research development proves the potential for continuous and further technological advancement of system-on-silicon LSI until 2020 through highly reliable, low-cost planar bulk technology.

This new breakthrough technology has provided NEC with a strong direction for future technological progress and transistor development, and it will continue to carry out aggressive R&D in this field toward the realization of next generation low-power, high-speed system LSI.

The results of this research will be announced at the international electron devices meeting (IEDM) being held in Washington D.C., U.S.A

from December 5 -7, 2005.

Source: NEC