IMEC reports CMOS integration of Hf-based dielectrics with Ni FUSI gates

December 7 2005

At today's IEEE International Electron Devices Meeting, IMEC announces a simple CMOS integration scheme of a NiSi gate for NMOS and a Ni2Si gate for PMOS on HfSiON with simultaneous 2-step silicidation. The potential of this novel integration process has been proven with ring oscillator demonstration. Alternative FUSI approaches such as adding Yb to Ni FUSI allowed further tuning of the work function to lower Vt, enabling dual gate CMOS technologies based on FUSI for (sub)-45nm.

FUSI gates are an interesting approach to overcome the incompatibility issues of poly-silicon gate electrodes with high-k gate dielectrics since the process is compatible with state-of-the-art poly-silicon front-end-of-line processing. At last year's IEDM and VLSI Symposium, IMEC published major progress on NiSi and Ni-rich Si (Ni2Si and Ni3Si) as FUSI candidates. The novel CMOS integration scheme for Ni FUSI gates on HfSiON, verified with a 41-stage ring oscillator demonstration, proves the potential of FUSI gates for (sub)-45nm node.

Doping, which has always been successful to set the work functions in conventional CMOS, appears to be ineffective for Ni FUSI gates and Hf-based dielectrics. However, NiSi has several phases that can be used to modulate the Vt. IMEC's novel integration scheme builds on the possibility to tune the work function by using different Ni-silicide phases (NiSi for NMOS and Ni-rich Si for PMOS) requiring different effective ratios of Ni- and Si thickness for NMOS and PMOS. Since silicides inherently have narrow line width effects, controlling the effective ratio

of Ni to Si thickness across all line widths is the key to successfully introducing this process in manufacturing. To achieve linewidth independent FUSI phase control, a 2-step FUSI process was developed with the same Ni thickness, but reducing the Si thickness on PMOS. The 2-step approach significantly reduces the amount of Ni available for reaction in narrow lines by selectively removing unreacted Ni prior to full silicidation of the gate.

The integration scheme offers several advantages:

· Simplicity since the same Ni deposition and silicidation process can be used for both NMOS and PMOS;
· Large process window for poly etch-back process: the same PMOS characteristics are obtained for a poly thickness variation of 50%;
· Dual work function and Vt tuning on HfSiON possible by phase control;
· Scalable, linewidth independent suitable Vt for both NMOS (0.5V) and PMOS (-0.3V);
· Solves process yield issues of Ni-rich silicides related to volume expansion, stress, filaments and voiding, resulting in a continuous silicide that is nicely confined between the sidewalls.

The high Vt of NMOSFETS based on Ni FUSI has been overcome by doping Yb into Ni FUSI. Yb doping allows to tune the work function of Ni FUSI from midgap (~4.72eV) to n-type band-edge (~4.22eV) which is compatible as a gate electrode for NMOSFETS with Vt down to 0.2V. No interface adhesion issues were observed as was found with work function modulation by other dopants such as As and Sb.

“We are pleased that over the last 2 years we’ve made considerable progress within our core program on one of the major bottlenecks in scaling CMOS beyond 45nm,” said Luc Van den hove, Vice President Silicon Process and Device Technology at IMEC. “Some concerns are

still remaining such as thermal stability, reliability and process control but the results show that FUSI is a leading candidate for successful integration of Hf-based dielectrics with metal gate electrodes for (sub)-45nm."

These results were obtained within IMEC's core program on sub-45nm CMOS, which joins forces from eight of the world's leading IC manufacturers - Infineon, Intel, Panasonic/Matsushita, Philips, Samsung, STMicroelectronics, Texas Instruments and TSMC.