

AMD, IBM Unveil New, Higher Performance, More Power Efficient 65nm Process Technologies

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In papers presented at the International Electron Devices Meeting (IEDM) in Washington, D.C., IBM and AMD today detailed their progress in bringing new, advanced semiconductor process technologies and materials to the 65 nanometer technology generation.

The companies announced that they have successfully combined embedded Silicon Germanium (e-SiGe) with Dual Stress Liner (DSL) and Stress Memorization technology (SMT) on Silicon-On-Insulator (SOI) wafers, resulting in a 40 percent increase in transistor performance compared to similar chips produced without stress technology, while controlling power consumption and heat dissipation.

The new process technologies reduce interconnect delay through the use of lower dielectric constant (lower-K) insulators, which can improve overall product performance and lower power consumption. In addition, the new technologies have shown ability to be manufactured at the 65nm generation and scaleable for use in future generations.

“Our joint work on developing advanced process technologies continues to ensure we can create and provide the highest performance, lowest power processors on the market,” said Nick Kepler, vice president of logic technology development at AMD. “Yet again, we can add another achievement to our list of successes that demonstrate how shared expertise and skills can result in overcoming roadblocks and creating

more valuable innovations for customers.”

Additional details about third generation strain technology innovations from AMD and IBM will be disclosed at the 2005 IEEE International Electron Devices Meeting, December 5-7, 2005 in Washington, D.C. This technology was developed as part of the AMD and IBM joint development alliance at AMD’s fabrication facilities in Dresden, Germany, and at the IBM Semiconductor Research and Development Center in East Fishkill, N.Y.

Source: AMD

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