

## IMEC launches industrial affiliation program to develop RF-CMOS for the 45nm era

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As part of IMEC's centralized research platform for sub-45nm CMOS technologies, the new IMEC industrial affiliation program (IIAP) on Analog/RF-CMOS for the 45nm era defines its goals to keep conquering the ITRS challenges. The program aims to develop process modules and device architectures to achieve RF CMOS performance at the 45nm node and to provide the necessary models for active and passive devices. The potential of the technology will be assessed through the benchmarking of circuit demonstrators.

To maintain a competitive position in the analog/RF domain, significant efforts are needed for a timely exploration and exploitation of analog/RF applications that will become available in future CMOS technology. Until now, there is no worldwide consensus for (sub)-45nm mixed signal technologies. An early assessment of the potential technologies for analog/RF CMOS applications is therefore mandatory to establish a long-term development strategy. To this end, IMEC launches a new IIAP, 45nm analog/RF CMOS, that strongly builds on the successful results of the preceding 90nm program.

The continued scaling opens perspectives for CMOS well beyond the 10GHz frequency range. The scaling will also allow for further reduction of power consumption for applications in the 1-10GHz range. However, at the same time, limitations start to appear, especially with respect to Vdd scaling and loss of analog performance with the introduction of new



materials. Also, the 45nm node (and beyond) is not well established for digital CMOS, which makes it more difficult to assess the analog/RF performance on the level of basic building blocks. The Analog/RF-CMOS IIAP has started beginning 2005 with an early assessment of the analog and RF performance of the different advanced process modules and device architectures. As a first result, a comparative study of planar MOSFETs versus FinFETs will already be presented at the IEDM conference in Washington at the end of this year. The second objective of the IIAP is to develop circuit topologies for 45nm Analog/RF CMOS that cope with the low Vdd operation and possible degradations of analog performance, with very high operating frequencies or with ultra low power consumption. The third objective is to provide circuit designers with state-of-the-art models of active and passive components for the 45nm analog/RF CMOS.

The IIAP builds on IMEC's multidisciplinary expertise in silicon process technology, packaging technology with focus on the integration of passive components and circuit design. The IIAP will run over 3 years. IMEC is in the process of recruiting additional partners for its new IIAP. Besides the traditional candidates such as IDMs, equipment and material suppliers, also fabless companies are invited to participate.

Source: IMEC

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