

Intel Developing Ultra-Low Power Manufacturing Process

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Additional 65nm Process Will Stretch Battery Life of Mobile Devices

Intel Corporation is developing an ultra-low power derivative of its high-performance 65 nanometer logic manufacturing process that will enable production of very low-power chips for mobile platforms and small-form factor devices. The ultra-low power process will be Intel's second process based on 65 nm process technology.

Intel's high-performance 65nm process provides both power consumption and performance benefits over Intel's current industry-leading 90nm manufacturing process. The company's new ultra-low power 65nm process provides Intel chip designers additional options in delivering the circuit density, performance and power consumption required by users of battery-operated devices.

"People typically embrace mobile platforms that maximize battery life," said Mooly Eden, vice president and general manager of the Intel Mobile Platforms Group. "Such products will be greatly enhanced by our new ultra-low power manufacturing process. We will design future mobility platforms to take full advantage of both leading-edge, 65nm manufacturing processes."

One of the factors in decreasing chip power consumption, which is important to mobile and battery-operated devices, is improving the design of the transistor. Lost electricity leaking from these microscopic transistors, even when they are in their "off" state, is a problem that is a

challenge for the entire industry.

"With the number of transistors on some chips exceeding one billion, it is clear that improvements made for individual transistors can multiply into huge benefits for the entire device," said Mark Bohr, senior fellow and director of Intel Process Architecture and Integration. "Test chips made on Intel's ultra-low power 65nm process technology have shown transistor leakage reduction roughly 1000 times from our standard process. This translates into significant power savings for people who will use devices based on this technology."

Intel's Ultra-Low Power 65nm Process Technology

Intel's ultra-low power, 65nm process technology includes several key transistor modifications which enable delivery of low power benefits while providing industry-leading performance. These transistor modifications result in significant reductions in the three major sources of transistor leakage: sub-threshold leakage, junction leakage and gate oxide leakage. The benefits of reduced transistor leakage are lower power and increased battery life.

About Intel's 65 nm Process Technology

Intel's 65nm processes combine higher-performance and lower-power transistors, a second-generation version of Intel's strained silicon, eight high-speed copper interconnect layers and a low-k dielectric material. Building chips using the 65 nm processes will allow Intel to double the number of transistors it can build on a single chip today (using Intel's 90nm technology).

Intel's 65nm processes will feature transistors measuring only 35nm in gate length, which will be the smallest and highest performing CMOS

transistors in high-volume production. By comparison, the most advanced transistors in production today, found in Intel Pentium 4 processors, measure 50nm. Small, fast transistors are the building blocks for very fast processors.

Intel has integrated a second-generation version of its high-performance strained silicon into these 65nm processes. Strained silicon provides higher drive current, increasing the speed of the transistors with only a two percent increase in manufacturing cost.

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