Fujitsu Introduces World-class 65-Nanometer Process Technology for Advanced Server, Mobile Applications

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Fujitsu Microelectronics America, Inc. today announced the availability of its 65-nanometer CS200 and CS200A series for ASIC and COT customers. The CS200 and CS200A, which were built using Fujitsu's leading-edge 65nm CMOS technology, offer the next step for SoC designers seeking improved performance as well as low power consumption.

The CS200 series is designed for high-end, high-performance server CPU devices and other advanced systems. Applications for the CS200A series include mobile products such as cellular phones, notebook computers, and other digital consumer products that require minimum power consumption. Both series offer maximum performance with minimum power consumption, and gate size reductions of 25 percent compared with the 90nm technology.

"Fujitsu's 65nm technology provides our customers with a complete set of options that enable them to maximize performance and minimize power consumption in their designs," said Keith Horn, senior vice president of sales and marketing for Fujitsu Microelectronics America. "The CS200 and CS200A series represent state-of-the-art technology for performance-oriented applications and mobile products that require long battery life."

The CS200 and CS200A series incorporate a range of transistors with

different leakage-power and performance points, so designers can mix transistor types to achieve both high performance and low power consumption. The CS200A technology provides an especially wide variety of transistors, ranging from low leakage for cellular phones to ultra-high speed for servers or network devices.

Gate Size Reduced 25 Percent Compared with 90-Nanometer CS100 Series

A major breakthrough in the new 65nm technology is size. Gate lengths of the CS200 and CS200A transistors are only 30 nanometers long, a 25 percent reduction compared with the transistor size in the Fujitsu 90nm CS100 series. The smaller transistors use a nickel polycide stack in place of the cobalt polycide/polysilicon stack used for the 90nm CS100 transistors. The lower sheet resistance of the nickel polycide ensures lower gate resistance, enabling higher speed.

"These improvements in transistor configurations and modified materials allow the 65nm CS200 transistors to exhibit superior speed and leakage characteristics," Horn said. "The result is a significant technological advance for our customers, reflecting Fujitsu's continuing leadership in world-class ASIC process technology."

There are other advances in the new 65nm technology. The CS200 and CS200A employ 11 copper interconnect layers instead of 10, making it easier to implement the most complex system-on-chip designs. The minimum pitch of the metal 1 interconnect layer is only 0.18µm, which allows a doubling of the gate wiring density compared with the 90nm CS100 series. To enhance performance and minimize power consumption further, Fujitsu uses advanced copper and porous Ultra Low-K (ULK) interconnect technology, which reduces parasitic interconnect capacitance.