Silicon Image Unveils Breakthrough Next Generation 6.0 Gb/s Serdes Technology

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Silicon Image, Inc.announced its next generation multi-rate MSLPhy™ Serializer/Deserializer (SerDes) technology, an integrated circuit transceiver that converts parallel data to serial data and vice-versa, capable of operating at bandwidths from 1.5 to 6.0 Gb/s. The MSLPhy is a low-cost solution for the storage market and other future mass markets with aggressive price/performance requirements. Silicon Image will be showcasing the 6.0 Gb/s SerDes technology during the Intel Developer Forum (IDF), being held August 23-25 at Moscone Center in San Francisco.

The next generation MSLPhy SerDes technology is capable of meeting multiple standards in the storage markets including Serial ATA (SATA) and Serial Attached SCSI. Combined with this week's introduction of Silicon Image's SiI 4723, the industry's first storage processor to offer 3Gb/s port speeds with hardware RAID, this announcement extends Silicon Image's leadership in high-speed serial technology for storage applications.

"Silicon Image continues to demonstrate leadership in silicon innovation," says Steve Tirado, Silicon Image's president and chief executive officer. "Being able to operate at 6Gb/s, the MSLPhy SerDes technology achieves a price/performance that is unmatched today and enables the continual evolution of the PC, CE and storage markets."

The continued demand for greater bandwidth is necessitating increases in SerDes speed. The new MSLPhy SerDes technology provides a next

generation, high-speed, serial, point-to-point link between devices and leverages much of the circuit innovation at the physical layer of Silicon Image's proprietary reduced overhead Multi-layer Serial Link (MSL) architecture. The MSL architecture is a robust, high-speed serial link IC technology that is key to achieving unparalleled price/performance. The MSL architecture includes a physical layer, coding layer and protocol layer, all on a single chip. Each of these layers is optimized for the particular application being addressed. By implementing the MSL architecture in low-cost CMOS technology, Silicon Image is able to deliver low-cost, high-bandwidth solutions for high-volume applications.

The next generation MSLPhy SerDes technology is implemented in standard 0.13 micron CMOS which offers high speed in a low-cost, robust design. The technology is critical for high-volume, mass markets and is also well suited to meet the needs of the PC, server and consumer electronics (CE) markets with aggressive price/performance requirements. Specific applications that benefit from this increased price/performance include direct attached storage (DAS) and network attached storage (NAS).

Silicon Image's market-leading implementations of the Digital Video Interface (DVI) and High-Definition Multimedia Interface (HDMI) standards for the display market, 2Gb/s Fibre Channel SerDes,1.5Gb/s and 3.0Gb/s Serial ATA, are also all based on this MSL architecture.