

# AMRC Developing Nano-Metrology to Probe Chip Structures at Atomic Level

August 17 2005

---

Engineers at the Advanced Materials Research Center (AMRC) in Austin are investigating a nanoscale approach to metrology that will allow them to examine new semiconductor structures at the atomic level, and so prepare the way for next-generation electronics.

The new methodology uses computer modeling designed for use with aberration-corrected transmission electron microscopy (TEM), an imaging method that can resolve as small as 0.7 Angstrom ( $\text{\AA}$ ). Many inter-atomic spacings in crystals, including silicon, have dimensions less than 0.1 nm ( $1 \text{ \AA}$ ).

This capability of viewing atom-sized structures will push forward the feasibility of advanced semiconductor structures such as fin-shaped field-effect transistors (FinFETs,) which are hoped-for replacements for conventional CMOS transistors that are running up against fundamental physical limitations.

“Aberration correction has changed the resolution of electron microscopy and opened new windows on the atomic structure of nanotechnology,” said Alain Diebold, a SEMATECH Senior Fellow and internationally recognized metrology expert. “By adding modeling, we can simulate images much more accurately, and truly understand what we are seeing.”

The AMRC project is being led by Dr. Brian Korgel, University of Texas at Austin chemical engineering professor, in consultation with

Diebold. Its aim is to employ unique software to simulate electron diffraction patterns of nanowires, whose diameters of less than 20 nm are similar to the dimensions of next-generation transistor gates and the fin-like structure of FinFETs. However, since nanowires are simpler structures, using them will allow researchers to refine their new microscopy techniques for more demanding metrology in the future.

“In the past, metrology has had trouble keeping up with the rapid advances in semiconductor scaling,” said Diebold. “Now we have a tool that gives us the potential to understand surface and interface morphology, and atomic structure, in ways that we have never been able to do before. It gives us a big leg up in understanding the structures of future devices.”

Citation: AMRC Developing Nano-Metrology to Probe Chip Structures at Atomic Level (2005, August 17) retrieved 19 April 2024 from <https://phys.org/news/2005-08-amrc-nano-metrology-probe-chip-atomic.html>

<p>This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.</p>
--