Texas Instruments Announces Next Generation PCI Express Physical Layer

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Expanding its broad portfolio of PCI Express products, Texas Instruments Inc. announces the third generation of its discrete PCI Express physical layer (PHY) chip. The new device, designed for flexibility and space savings, is targeted at interfacing with ASICs as well as low cost FPGAs in PC add-in cards, communications, test equipment, servers and other embedded system applications.

TI has designed the new PHY to be compliant to PCI Express 1.1 specifications, which is critical for interoperability with other PCI Express applications. The new device is based on TI's proven test chip that has been demonstrated at numerous trade shows and is also used in TI's PCI Express 1394a and PCI Express bridge technologies that are available today.

The TI PCI Express PHY gives board designers flexibility by offering both an 8 bit and 16 bit interface. The interface also is based on the PHY Interface for the PCI Express (PIPE) Architecture version 1.0 from Intel, with minor enhancements that allow for lower power consumption and a simplified interface for easy integration.

"The PCI Express PHY is the foundation of all PCI Express applications, and we see a strong transition to PCI-Express across multiple market segments," said Brian Whitaker, marketing segment manager, computer connectivity solutions, TI.

Samples of the PCI Express PHY will be available in the second half of

2005 and TI will price the device to enable low cost PCI Express ASIC and FPGA solutions in the market.