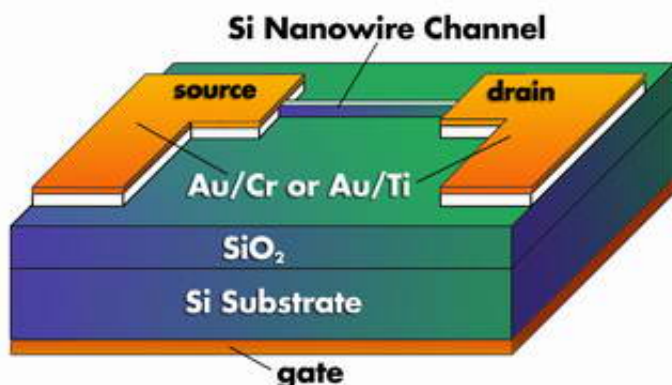


New design developed for silicon nanowire transistors

July 1 2005



In an advance for nanoscale electronics, researchers at the National Institute of Standards and Technology (NIST) have demonstrated a new design for silicon nanowire transistors that both simplifies processing and allows the devices to be switched on and off more easily.

Image: A schematic diagram of the NIST nanowire transistor.

The NIST design, described in a paper published June 29 by the journal *Nanotechnology*,* uses a simplified type of contact between the nanowire channel and the positive and negative electrodes of the transistor. The design allows more electrical current to flow in and out of the silicon. The researchers believe the design is the first to demonstrate

a "Schottky barrier" type contact for a nanowire transistor built using a "top-down" approach. This barrier, an easily formed metal contact that electrons can tunnel through, requires much less doping with impurities than do conventional ohmic contacts, thereby simplifying processing requirements. Schottky contacts also offer more resistance and restrict electrical flow to one direction when the transistor is off.

In the NIST transistor design, the 60-nanometer-wide channels exhibit a much greater difference in current between the on and off states than is true for larger reference channels up to 5 micrometers wide. This suggests that when a channel is scaled down to the nano regime, the ultra-narrow proportions significantly reduce the current leakage associated with defects in silicon. As a result, the transistors are less sensitive to electronic "noise" in the channel and can be turned on and off more effectively, according to the paper's lead author, Sang-Mo Koo, a NIST guest researcher.

Silicon nanowire devices have received considerable attention recently for possible use in integrated nanoscale electronics as well as for studying fundamental properties of structures and devices with very small dimensions. The NIST work overcomes some key difficulties in making reliable devices or test structures at nanoscale dimensions. The results also suggest that nanowire transistors made with conventional lithographic fabrication methods can improve performance in nanoscale electronics, while allowing industry to retain its existing silicon technology infrastructure.

*S.M. Koo, M.D. Edelstein, Q.Li, C.A. Richter and E.M. Vogel. 2005. Silicon nanowires as enhancement-mode Schottky barrier field-effect transistors. *Nanotechnology* 16. Posted online June 29.

Source: NIST

Citation: New design developed for silicon nanowire transistors (2005, July 1) retrieved 19 April 2024 from <https://phys.org/news/2005-07-silicon-nanowire-transistors.html>

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.