

# Reference Materials Planned for Semiconductor Industry

July 1 2005

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Companies and research organizations are invited to collaborate with the National Institute of Standards and Technology (NIST) and SEMATECH in the development and evaluation of a new generation of reference materials for the semiconductor and tool manufacturing industries. The work is a continuation of NIST's efforts to provide standard "rulers" for measuring chip features. The new reference materials will differ from the previous generation in several ways. Current plans call for each reference material to be configured as a 200-millimeter wafer with a selection of die sites, each with multiple test structures with certified critical dimensions between 40 and 500 nanometers.

The reference-material design, fabrication and calibration will be led by the NIST-SEMATECH team. The principal role of participating companies and other organizations will be evaluation of the reference materials, but they also may contribute expertise, equipment time, or other resources. Participants will receive one or more wafers, and all associated measurement documentation, on completion of the work.

Those interested in participating are invited to a public event scheduled for July 13, 2005, at the San Francisco Marriott. More information and registration forms are available online at [www.sematech.org/membersite/MServlet?mtgId=7682](http://www.sematech.org/membersite/MServlet?mtgId=7682). For further information contact, Michael Cresswell, michael.cresswell@nist.gov, (301) 975-2072.

Information about the previous set of reference materials, delivered to SEMATECH member companies earlier this year, is available at [www.physorg.com/news3177.html](http://www.physorg.com/news3177.html)

Source: NIST

Citation: Reference Materials Planned for Semiconductor Industry (2005, July 1) retrieved 24 April 2024 from <https://phys.org/news/2005-07-materials-semiconductor-industry.html>

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