0.4-V DRAM array technology using twin cells for next generation mobile devices

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Enabling the longer retention time and fast read/write operation under low voltage condition

Hitachi, Ltd. in cooperation with Elpida Memory, Inc., have proposed a new DRAM (*1) circuit design enabling 0.4-V operation. The proposed array employs a twin cell scheme, which uses two conventional DRAM cells to store 1-bit information, and achieves a longer retention time and fast read/write operation under low voltage condition. This technology will be fundamental for designing DRAM, with its large memory capacity, as the low power memory device in next generation mobile information devices.

Memory devices used in mobile information devices need to be able to provide both memory capacity to support increasing new functions and contents, as well as low-power consumption, in order to extend battery life. SRAM (*2) is currently the main memory device used in cellular phones, due to its low power consumption features. There are, however, several issues for its use in future mobile information devices, such as its large cell size which places restrictions on increasing capacity, and the limitation on lowering the operation voltage due to memory cell variation. DRAM, in contrast, is suited to increasing capacity, and is already being employed as the memory device in some mobile devices. The hurdle to the wider employment of DRAM, however, is low power consumption, and issues such as the shortening of data retention time when the voltage for recording in the memory cell (bit-line voltage) is decreased, and the high control voltage required for the memory cell

transistor (word-line voltage), exist.

To overcome these problems, Hitachi and Elpida proposed a new DRAM circuit for a low power DRAM using a twin-cell scheme. Features of the proposed DRAM are described below:

1. Lowering bit-line voltage while ensuring retention time
A twin cell scheme, which uses two conventional DRAM cells for storing 1-bit information, was employed. It was found that with the twin cell scheme, the bit-line voltage could be reduced while maintaining the retention time of a conventional single cell.(*3) Simulation results indicated a retention time as long as that for a single cell array at 1.0V, could be achieved at 0.4V, and thus, the power consumption of the DRAM memory array can be decreased by about 60%.

2. Lowering word-line voltage using a plate-driven twin-cell array
In a conventional DRAM array, a high word-line voltage is required to store enough signal charge for '1' information in a memory cell capacitor. As the signal charge for '1' information can be halved using the twin cell array and plate-driven scheme, the word-line voltage can also be reduced.(*4) Simulation results indicated that the word-line voltage could be decreased from 3V to 1.8V, using the twin cell and plate driven schemes, and thus, the power consumption in the pumping circuit for the word line voltage can be reduced by about 70%.

This new technology realized improvement in retention time and fast read/write operation under low voltage conditions. Simulation results indicated that the power consumptions of the memory cell array and the word-line voltage generator, are reduced by 60% and 70%, respectively, compared with conventional DRAM, respectively. This technology is expected to be fundamental circuit technology for employing high density RAM as a low power memory in next generation mobile information devices.

These results were presented on 18th June 2005 at the Symposium on VLSI Circuits, held in Kyoto, Japan from 16th - 18th June 2005.

Technical Terms:

(*1) DRAM: Dynamic Random Access (read/write) Memory which requires a periodic refresh operation to maintain data. Each memory cell consists of one (MOS) transistor and one capacitor to store one bit (binary data).

(*2) SRAM: Static Random Access Memory does not require a periodic refresh operation as in DRAM to retain data, instead a constant and sufficient power supply voltage is required to indefinitely retain data.

(*3) With the twin cell scheme, one of two memory cells stores '1' information and the other stores '0' information. In the read operation, the difference in charge between the two memory cells is read. Thus, the influence of leakage current is smaller in a twin cell scheme as compared to that in a single cell array. As a result, it was found that the retention time of the twin cell array became more than 3 times longer than that of a conventional single cell array.

(*4) By writing both '1' and '0' information in each memory cell, the necessary charge to read the '1' information can be reduced, thus the word-line voltage can also be reduced. Further, by operating the plate (the common electrodes of the capacitor) without a dummy cell (required in a plate driven scheme for a single cell array), the '1' information can be written sufficiently despite a decrease in word-line voltage in the twin-cell array.