UMC's Researchers Extend Traditional Nitrided Gate-oxide to beyond the 65nm node

June 16 2005

Nitrogen profile engineering used to downscale effective oxide thickness towards 1nm to improve semiconductor performance

UMC, a world leading semiconductor foundry, today announced that its research and development team has achieved a significant engineering milestone by shrinking the Equivalent Oxide Thickness (EOT) of nitrogen doped silicon oxide (Oxy-nitride, SiON) gate dielectrics to approximately 1.0 nm using a new nitrogen profile engineering technique. This accomplishment allows more aggressive scaling of transistors to enhance overall semiconductor performance without the introduction of new materials.

"UMC's R&D team is continually developing new and innovative solutions to overcome ever-emerging challenges brought by advanced process technology," said S. F. Tzou, director of UMC's Advanced Module Development Division. "This latest achievement demonstrates that our nitrogen profile engineering technique can be used to improve performance at 65nm. This success also gives us confidence in the viability of extending SiON gate dielectrics for future CMOS applications beyond 65nm."

The novel SiON gate dielectric processing technique, unveiled by UMC engineers, enables the precision positioning of the nitrogen doping profile as well as accurate control of thickness. UMC engineers used a less than 3% nitrogen atomic concentration layer near the bottom Si-substrate / SiON interface, while using a higher concentration of

nitrogen at the top interface of the poly silicon gate/SiON gate dielectric. The newly achieved effective oxide thickness of ~1.0 nm exhibits a gate leakage current of less than 10A/cm2 with improved PMOS threshold voltage stability, lower interface state density, and resistance to boron penetration. The enhanced mobility also signifies higher performance and process reliability at the same time.

Scaling down the conventional oxy-nitride to below 1.2nm of EOT typically results in the rapid escalation of gate leakage current. The use of a heavier nitrogen concentration, a favored method to reduce leakage, typically induces undesirable side effects such as mobility degradation and threshold voltage shift. Thus, this approach is not ideal for practical use. New high-k gate dielectric materials associated with metal gate electrodes have also been proposed to alleviate this barrier, though these inevitably come with new challenges of their own: namely, carrier mobility degradation, unacceptable threshold voltage instability, and dual work-function metal gate integration issues, etc. that would require intensive and costly research efforts to address.

Oxy-nitride, which has been used for decades in semiconductor manufacturing for legacy process technology generations, has remained a viable candidate, but only if a proven means could be implemented to suppress escalation of the gate leakage current while reducing thickness. Traditionally, increased power consumption due to leakage has been viewed as a trade-off with lower EOT to gain more speed. UMC has demonstrated through its new nitrogen profile engineering technique that existing oxy-nitride can be used to achieve greater transistor performance without having to sacrifice power consumption.

The details of this technology finding were reported in the Symposia on VLSI Technology and Circuits held at Kyoto, Japan on June16, 2005.