Ultra-Dense SRAM cell in 45-nm Low-Cost, Low-Power Conventional Bulk CMOS Technology

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The Crolles2 Alliance today presented a paper* describing the creation, under production conditions, of six-transistor SRAM-bit cells with an area less than 0.25 square microns – half the size of earlier solutions – using conventional bulk CMOS technology and 45-nanometer design rules.

Crolles2 is the R&D alliance of Freescale Semiconductor, Philips and STMicroelectronics. The 1.5-Mbit arrays were produced at the Alliance's 300-mm wafer fabrication pilot line in Crolles, France. The joint paper underscores the continued success of one of the industry's largest research and development alliances leading at the 65-nm and 45-nm CMOS design nodes.

"Building upon our history of innovation and technology leadership, we have successfully demonstrated the feasibility of producing functional circuits and ultra-dense SRAM cells at the 45-nm node," said the three Alliance chief technology officers: Claudine Simson, Freescale Semiconductor; Rene Penning de Vries, Philips Semiconductor; and Laurent Bosson, STMicroelectronics.

The advanced Crolles2 wafer fabrication line is already running pilot production of 90-nm CMOS devices on 300-mm wafers and is on target to prototype 65-nm CMOS during 2005. The new achievements at 45 nm are seen as a vital stepping stone towards future-generation high-

volume process technologies.

Meeting the Power Challenge of Nanometer Geometries

Semiconductor industry customers continuously expect smaller, more highly integrated devices with greater performance and lower power consumption. To meet this demand, semiconductor manufacturers continuously push for smaller geometries, which creates new complexities and manufacturing challenges.

With each new generation of process technology, engineers have typically reduced area by a factor of two. But as process geometries are reduced and oxide layers get thinner, the control of leakage currents becomes a greater challenge. It is a particularly important factor in CMOS devices designed for battery-powered products such as mobile phones and MP3 players.

To meet this challenge, the Crolles2 Alliance is evaluating the extension of conventional CMOS process technology to produce SRAM cells at 45 nm while achieving the necessary cell and transistor performance. Building on its experience at 90 nm and 65 nm, Alliance engineers have developed a process that uses existing materials and process flows, maximizing the re-use of technology modules. Scientists at Crolles also are evaluating other solutions, including metal-gate technology and the use of high-k dielectric, which are technically more complex and less mature than standard CMOS logic processes.

Capitalizing on Previous 45-nm Accomplishments

The Alliance previously demonstrated the feasibility of using conventional architecture to design transistors for 45-nm low-cost

applications, as reported in a paper presented at IEDM 2004 (IEEE International Electron Devices Meeting). The initial strategy was to control gate leakage by limiting the scaling of the gate oxide while other features were scaled down, and to compensate subsequent performance loss by the use of process-induced strained silicon.

Now this principle is being extended to the fabrication of functional sub-0.25-square micron six-transistor SRAM-bit-cells as a practical demonstration of high-density integration. The Alliance used maskless lithography (e-beam) for critical levels to speed-up realization and to minimise costs in the development phase. The process technology is, however, fully compatible with the optical lithography that will be used in 45-nm CMOS production. These functional 45-nm SRAM bit-cells validate the concept of producing very high density features using low-cost wafers in a conventional process flow.

* “0.248µm2 and 0.334µm2 Conventional Bulk 6T-SRAM bit-cells for 45nm node Low Cost – General Purpose Applications”

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