STMicroelectronics Pioneers Major Breakthrough in SoC Design

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Five years of research and development at STMicroelectronics are today revealed by the publication of a book on a novel chip design methodology. In their efforts, the authors of *'Transaction Level Modeling with SystemC'* have pioneered the next practical level of abstraction for production digital designs, yielding significant improvements in productivity and first-time silicon success. This modeling concept is supported by the newly released TLM library standard by the Open SystemC Initiative (OSCI), introduced at this year's Design Automation Conference in Anaheim, California (June 13-17, 2005).

The increasing complexity of Systems-on-Chip (SoCs), and the growing proportion of embedded software, is calling for new design methodologies. Transaction-Level Modeling bridges the gap between design productivity and process capacity by raising the level of abstraction in specifying and modeling an SoC design. The book, *'Transaction-Level Modeling with SystemC,'* authored by an advanced R&D team from STMicroelectronics, presents an industry-proven approach to resolve critical system-level issues in today's complex digital designs.

ST's TLM solution, based on the open-source SystemC modeling language, has been proven to strike the right balance between abstraction and accuracy, efficiently accommodating early embedded software development, functional verification, and performance analysis. Employed as the executable functional specification to compare against the Register-Transfer-Level (RTL), un-timed TLM models are also

assembled to build virtual prototype to develop significant software in parallel with hardware design. When complemented with timing information, the same models serve the needs of architecture analysis to ensure the compliance of an SoC design with real-time constraints of the targeted application.

Beyond these benefits, the new abstraction level also provides a single functional reference that is shared between software, hardware, and system-level engineers. Sharing this executable specification removes ambiguity, duplication of information, and most importantly, helps to detect architecture flaws before the cost of modification becomes too high. These capabilities allow reduction in design times up to 50 % over previous methodologies and help prevent silicon re-spins.

“We are witnessing a real paradigm shift in the way software and hardware engineers work with each other,” said Philippe Magarshack, Group Vice President of Central R&D at STMicroelectronics. “TLM allows us to deliver a prototype to customers before the RTL is frozen and therefore cuts time to market on a previously unattainable scale.”

‘Transaction-Level Modeling with SystemC’ (ed. Frank Ghenassia) published now by Kluwer Publishing, discusses solutions to enhance existing system-level methodologies, offers modeling guidelines, and helps IP suppliers provide TLM views of their components.

SystemC is an interoperable modeling platform which provides hardware-oriented constructs within the context of C++ as a class library implemented in standard C++. Its use spans design and verification from concept to implementation in hardware and software.
The Open SystemC Initiative (OSCI) is an independent not-for-profit organization composed of a broad range of companies, universities and individuals dedicated to supporting and advancing SystemC as an open source standard for system-level design.