Renesas and Hitachi Develop High-Speed Programming Technologies for Multilevel AG-AND Flash Memories

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Renesas Technology Corp. and Hitachi, Ltd. today announced that they have co-developed two high-speed programming technologies for AG-AND (Assist Gate-AND) flash memory*1 devices, high-speed data storage built with multilevel*2 cell technology. Details of these new technologies are presented at the 2005 Symposia on VLSI Technology and Circuits, an international conference on LSI devices and circuits that opened in Kyoto, Japan on June 14, 2005.

The new developments comprise (1) a memory cell operation technology that boosts the efficiency of hot electron injection by a factor of 20 during programming and (2) a multilevel, high-speed programming circuit technology that reduces the overhead associated with multilevel programming. The circuit technology has been applied to Renesas' 4-Gigabit AG-AND flash memories (90-nanometer process technology), which are now in volume production.

Both of the newly developed technologies offer potential as basic techniques for achieving high-speed, multilevel storage in AG-AND flash memories of the 90 nm generation onward.

High-density flash memory is rapidly permeating our lives as data storage memory, used in devices such as digital cameras, mobile phones, and silicon audio players, as well as USB memory. Next-generation flash memory cards that store high-quality moving picture data in a small,

lightweight form will require significantly higher density and faster programming speeds to handle data downloads efficiently.

In response to these needs, Renesas developed jointly with Hitachi a first-generation AG-AND flash memory in 2001. That device offered a smaller cell area together with the industry's fastest multilevel programming speed of 10 MB/s for 1-Gigabit products that use a 130-nanometer process. In 2003, the companies also developed a memory cell technology for second-generation AG-AND flash memory devices. This technology achieves a 10 MB/s programming speed and significantly reduces the memory cell area for 4-Gigabit products that use a 90 nm process.

While the use of hot electron injection programming*3 in AG-AND flash memory enabled a fast programming speed at a low voltage, the efficiency of hot electron injection needed to be improved to realize a fast programming speed of 10 MB/s in a 4-Gigabit part. A speed problem also occurred as the process rule reaches 100 nm or less.

To cope with this challenge, Renesas Technology and Hitachi have jointly developed a new memory cell operation technology and circuit technology enabling faster programming of multilevel AG-AND flash memories.

The features of these newly developed technologies are summarized below.

(1) Memory cell operation technology increases the efficiency of the hot electron injection programming method
The previous 0 V source voltage used in memory cell programming has been made negative, strengthening the field in both the vertical and horizontal channel directions, and improving the hot electron generation rate and electron attraction rate into the floating gate. As a result, the

electron injection speed has been increased by a factor of 20 compared with the previous use of a 0 V source voltage.

(2) High-speed programming circuit technology resolves the multilevel programming overhead problem
This circuit technology*4, representing an improvement of the original constant-charge-injection programming technology*5 used in 1-Gigabit products, performs programming by switching the bit line capacitance used in electron injection according to the levels within the multilevel technology. This reduces the overhead associated with programming of the highest level, and provides fast, uniform programming.

Verification tests of the new memory cell operation technology (1) above were made using a 90 nm process test device. Results showed that the hot electron injection time needed for an actual programming operation was reduced from 2 microseconds to less than 100 nanoseconds. Also, the high-speed programming circuit technology (2) above was applied to Renesas' 4-Gigabit AG-AND flash memory products. Test data revealed that the programming operation overhead decreased by 10% compared with the conventional technology.

Notes:
(1) AG-AND flash memory: An original memory cell structure employing a field isolation method comprising alternating assist gates (AGs) that prevent inter-cell interference and floating gates. Programming can be implemented by hot electron injection using a small channel current, and the cell area can be made smaller than with the conventional shallow-groove isolation method in which cells are isolated by forming grooves.

(2) Multilevel cell technology: A technology suitable for high-density flash memory, effective in reducing chip size, whereby four or more values, such as 00, 01, 10, and 11, can be held as opposed to the usual

two values, 0 and 1, of ordinary memory. When four values are used, one cell does the work of two ordinary cells.

(3) Hot electron injection programming: A programming method whereby high-energy "hot" electrons accelerated by a channel electric field are injected into a floating gate. The memory cell programming time (electron injection time) is 10 Âμs or less, an order of magnitude faster than with the conventional tunnel programming method.

(4) With the conventional constant-charge-injection programming technology, all levels in the multilevel arrangement are programmed using the local bit line capacitance. With the new circuit technology, highest-level programming is performed by switching to the global bit line, and mid-level programming by switching to the conventional local bit line.

(5) Constant-charge-injection programming technology: A programming technology that achieves fast and uniform programming characteristics by causing only a fixed charge amount stored beforehand in the bit line capacitance to flow in hot electron injection programming.