NEC Develops Highly-Reliable CMOSFET with Phase Controlled NiSi (NFET) & Ni3Si (PFET) Gate Electrode

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NEC Corporation ("NEC") today announced the development of a transistor featuring a new gate stack structure using a hafnium ("Hf")-based, high-k dielectric and a metal gate electrode, which simultaneously realize significant gate leakage suppression and improvement in transistor operation speed. The newly developed metal gate/high-k structure is stable even through the conventional CMOS manufacturing process and realizes transistor life time of up to 10 years with practical usage presumed at 85oC.

This result was mainly enabled by the following:

(1) Suitable threshold voltage ("Vth") was realized for both PMOS and NMOS based on the composition control of Hf in the dielectric film and Ni in the electrode. NiSi and Ni3Si electrodes were formed on HfSiON with 50% Hf/(Hf+Si) composition for NMOS and PMOS, respectively.

(2) The NMOS and PMOS with a new gate stacked structure realize reduction of leakage current, improvement in sub-threshold current, and carrier mobility. The result is an improvement in transistor current drivability by 28% for NMOS(NiSi) and 52% for PMOS(Ni3Si). In addition, the reliability of NEC's gate stack structure ensures 10 years of practical usage in a presumed environment of 85oC.

A simple phase controlled Ni full silicide ("Ni-FUSI") formation method

enables good thermal stability of the gate stacked structures of Ni-FUSI/high-k even through the conventional CMOS manufacturing process. This structure also ensures the feasibility of up to 45nm-node low standby power ("LSTP") and low operation power ("LOP") transistors.

In recent years, the demand for LSI scaling technology to achieve power devices boasting higher speed and lower power is increasing. With this trend, the gate SiO_2 layer, now typically thinned down to less than 2nm, suffers from a rapid increase in direct tunneling current, which leads to an increase in device power consumption. As a result, ways to suppress the gate leakage are being studied intensively. In 2003, NEC demonstrated the operation of CMOS circuits with Poly-Si/HfSiON as a gate stack module in addition to establishing reliability technologies for it.

However, with further improvement in operation speed and consumption power in advanced LSIs, degradation of current drivability is becoming a progressively serious issue due to poly-Si gate depletion. Now, the use of metal gate electrodes in place of poly-Si is being considered as a promising solution to this issue, and intensive development in this area of research is now under way worldwide. In 2004, NEC and NEC Electronics also researched and developed metal gate electrodes to apply onto high-k gate dielectrics for future advanced LSIs. Their developed gate stack structure using Ni silicide metal gate and HfSiON gate dielectrics achieves elimination of gate depletion. Furthermore, while based on the simple production process of full silicidation, a novel approach of forming the electrodes with different Ni/Si composition ratios for PMOS and NMOS, respectively, provides a wide range of Vths for both types of transistors.

However, the following challenges have been noted:

-- It is difficult to adjust the suitable threshold voltage for both NMOS and PMOS transistors with the Ni-FUSI gate because the mechanism for effective work function control of Ni silicides on high-k gate(HfSiON) is unclear.

-- The long term reliability of Ni-FUSI/high-k MOSFET with practical usage under an electrical stress condition, as well as the thermal stability of this gate stack structure in the conventional CMOS process are still unclear. Both are very important factors for product manufacturing.

NEC has clarified that the Ni/Si composition of the gate electrode and the Hf/Si composition of the HfSiON gate insulator are the important parameters for obtaining suitable CMOS Vths. The amount of Hf-Si bonds at the gate/insulator interface is the key parameter to control the Vth. The NiSi and the Ni3Si electrodes on 50%-Hf and HfSiON-composed film realize suitable Vth with tight distribution for both NMOS and PMOS, respectively. NEC has also confirmed that this gate stack structure possesses good thermal and electrical stability. The newly developed gate stack structure using Ni silicide metal gate and HfSiON gate dielectrics achieves elimination of gate depletion and leads to notable improvement in both gate leakage and transistor operation speed. This device also realizes stable current output after prolonged operation. NEC's research result is considered a large step toward the realization of low-power-consuming devices using metal/high-k gate stack structure.

If this technology is installed in the latest slim devices and applied to mobile equipment such as mobile handsets, which are vital to a ubiquitous networked society, production of high-speed SOC without shortening of the battery life span will be enabled, contributing to the spread of highly reliable mobile devices.

NEC will accelerate research and development efforts of this high-k gate insulator, working toward the provision of highly reliable mobile

terminals for a ubiquitous networked society.

Source: NEC

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