IMEC to create solutions for sub-45nm CMOS scaling

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Together with its CMOS core partners, IMEC will announce several research breakthroughs on new gate-stack technologies and multiple-gate FET (MuGFET) devices at the 2005 Symposium on VLSI Technology. A combination of advances in MuGFETs and gate-stack technology paired with lithography improvements also resulted in a new record for a fully working 6-transistor SRAM cell of just 0.274μm^2 in area.

"The results presented at VLSI 2005 show that IMEC and its core partners have made significant advances in developing the generic process steps, modules and devices for continued scaling below the 45nm node," said Luc Van den hove, Vice President Silicon Process and Device Technology at IMEC. "By combining the expertise of all partners, our program has gained a momentum demonstrated in the record of papers at VLSI 2005."

As CMOS devices continue to scale, short channel effects start to dominate, leading to higher leakage and performance degradation. In IMEC's core program, new device architectures such as triple-gate transistors and new gate stacks are investigated to overcome this.

Paper Topics

Fully silicided gates scalable to 30nm gate length

IMEC will demonstrate for the first time the scalability of fully silicided

(FUSI), nickel silicide gates to 30nm gate lengths. FUSI gates are an interesting approach to overcome the incompatibility issues of poly-silicon gate electrodes with high-k gate dielectrics since the process is compatible with state-of-the-art poly-silicon front-end-of-line processing.

High-performance NMOS transistors using HfO2/TaN gate stack

A breakthrough has been achieved in high-performance NMOS transistors with a HfO2/TaN gate stack using a low thermal budget process called SPER (solid-phase epitaxial regrowth). A 2x-improvement in mobility over previous low-thermal (gate-last) results has been achieved. Drive currents as high as 815µA/µm at Ioff of 0.1µA/µm has been obtained resulting from a high mobility and low Vt that is caused by the lower capacitance-equivalent oxide thickness of the transistor in inversion.

MuGFETs with metal gates and strain

IMEC will present several advances in MuGFET devices. MuGFETs are potential candidates to replace planar MOSFETs for specific applications in the 32nm node and beyond due to their excellent control of short channel effects and consequently intrinsic better scalability.

Two methods to be presented are based on the combination of non-doped fins with metal gates, which have proven their potential to solve the threshold voltage tuning problem in MuGFETs. A CMP-less approach for the integration of fully silicided gates in FinFETs has been developed that enables simultaneous silicidation of the gate, source and drain without increasing the source/drain resistance.

For the first time, TiN metal gates and HfO2 gate dielectrics have been integrated in NMOS and PMOS triple gate devices with fin widths down to 10nm. By using a metal gate, the threshold voltage of both NMOS and PMOS devices could be successfully set.

Recessed strained SiGe has been successfully introduced in the source and drain regions of PMOS MuGFET devices, improving the on-state current by 25%. The use of recessed strained SiGe in the source and drain regions of planar silicon PMOS devices has previously demonstrated a 35% improvement in drive current. The introduction of uniaxial compressive stress along the channel has for the first time now been proven to be beneficial for MuGFETs. Ten-to-15 percent of the improvement can be attributed to a decrease in series resistance, while the remaining part results from the strain enhancement of the transport characteristics.

Record in 6 transistor, triple-gate SRAM cell with metal gates

IMEC's 6-transistor SRAM cell based on MuGFETs, which was described at the December 2004 International Electron Devices Meeting (IEDM), has been further scaled to a cell size of only 0.274µm2. This feat was accomplished by using lithography process optimizations and insertion of metal gates (TaN). The gate length of the devices is a miniscule 37nm. This result shows the potential of MuGFETs with metal gates for further scaling below the 45nm node.

Because of IMEC's longstanding expertise in semiconductor research three-to-10 years ahead of industrial needs, Dr. Gilbert Declerck, president and CEO of IMEC, has been invited to present a look at the future of nanoelectronics as an invited talk in the plenary session. Dr. Declerck asserts that if technologists can manage the giga-complexity of

the ‘More Moore’ world and show ultra-creativity for the ‘More than Moore’ world, then they can develop networked computing and communication devices that will help humans reach their potential.