IBM to Offer 'Statistical Timing' Solutions for Chip Designers

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IBM today announced it would market to companies that design advanced integrated circuits a new suite of technology solutions aimed at greatly improving the performance of their chip designs.
It is a statistical timing analysis solution created from IBM's EinsTimer suite. Now, for the first time, this design solution will be offered commercially through IBM Engineering & Technology Services (E&TS).

"Process variability is becoming harder to analyze and EinsTimer statistical timing analysis will enable designers to better understand their design sensitivities," said Anthony Yu, Vice President, E&TS.

As scaling for chips used in a wide variety of computing and networking systems proceeds to finer and finer geometries -- 90 nanometers and below - - enhanced electronic design automation "flows" such as these statistical timing solutions are needed to help reduce risk, improve flexibility and help get products to market faster.

Dealing with Variability

This software offering provides support for industry standards (e.g., sdc, .lib, spef) and will help designers deal with variability in a comprehensive manner. "Variability in digital integrated circuits makes timing verification an extremely challenging task," added Dale Hoffman, Director of Business Development and Chief Technical Officer, E&TS.

"IBM's knowledge of deep submicron physics, chip manufacturing, lithography, design flows and EDA tools have been leveraged to offer this comprehensive solution."

IBM's ASICs teams have been using statistical methods in 90 nanometer ASICs designs. These methods aid in separating different components of variation and using statistical techniques giving credit to critical paths for certain types of variation, thus removing conservatism. Since the design optimization engine also uses the same timing model and timing engine, this tight integration may allow for faster timing closure and results in a more optimized and robust design.

EinsTimer statistical timing -- pioneered by IBM Research -- has incremental statistical timing analysis capability, including support for front-end, back-end and environmental variations.

For Aggressive Designs

This solution allows efficient coverage of the entire process space in a single static timing analysis with reduced timing pessimism. EinsTimer statistical timing also includes support for several diagnostics including the sensitivity of all timing quantities to process variables, important measures of the robustness of a circuit.

For aggressive designs, the timing analysis can be used to generate a yield curve in order to help facilitate performance vs. yield trade-offs. The timer can also be used in a physical optimization flow to take advantage of incremental statistical timing. The result can be higher performance, more robust timing closure and simultaneous coverage of all corners of the process space during optimization.

EinsTimer statistical timing solutions are available immediately. IBM representatives will demonstrate EinsTimer statistical timing from June

13 to 16 at DAC conference in Anaheim, CA.