New Concept for Novel Low-k Film Compatible with 45nm-node LSI Interconnects

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NEC and MIRAI Project today announced the joint development of a low dielectric-constant (low-k) film, which is realized through a newly developed concept, and is expected to lead to power reduction in advanced LSIs. The low-k film contains very tiny, molecular-scale pores introduced by a newly developed novel molecular-pore-stacking ("MPS") technique. Its feasibility to ultrafine copper interconnects in future 45nm-node LSIs has been confirmed, achieving double the interconnect density as that of 65nm-LSIs and a 16% reduction in interconnect parasitic capacitance, which is essentially the source of active power consumption.

Characteristics of the new technology are as follows:

(1) A new MPS process had been developed, in which porous low-k film is formed by the direct stacking of silica-based precursor molecules, each containing a sub-nanometer pore as its molecular structure. This process successfully realizes low-k film with a desired dielectric constant of 2.4 for 45nm-node LSIs.

(2) Achieving double the interconnect density as compared to that of 65nm-node LSIs due to the excellent insulating properties of the MPS low-k film, and a 16% reduction in interconnect parasitic capacitance mainly due to its low-k characteristics, its feasibility as an insulating dielectric for ultrafine copper interconnects in future 45nm-node LSIs

(70nm spacings) has been verified.

(3) In 70nm-spaced lines, the MPS low-k film was confirmed to possess the same level of insulation reliability as that of conventional 65nm-node LSIs with conventional porous low-k film (k=2.6) in 100nm-spaced lines. It has also been shown that by employing a pore seal ("PS") structure with NEC's original insulating layer that was formed by a plasma-polymerization process, the insulation reliability is further improved by a factor of five due to the covering of the etched surfaces of the MPS low-k film.

It is expected that this MPS technology will realize a reduction in size and active power consumption of next-generation digital information processors for applications such as high-speed servers and multi-functional mobile terminals.

When the integration density and the operation speed of LSI devices increase, it is inevitable that their power consumption will also eventually increase. As it is vital to realize the reduction of power consumption from an economic and ecological point of view, researchers worldwide have been continually striving to develop breakthrough technology to achieve this goal. One of the considerable factors in power consumption arises from the LSI interconnects as a consequence of the rapid increase in the number of interconnected nodes in addition to the growing total length of interconnects in scaled-down chips in each new generation. In other words, it is vital to reduce interconnect parasitic capacitance in order to reduce power consumption. To this end, low-k film is a key material in the narrow-spaced interconnects in LSI chips as it prevents undesired increases in parasitic capacitance. For 45nm-node LSIs the dielectric constant is desired to be lower than 2.5, however this is currently difficult to achieve with conventional low-k material/process technology.

NEC has been striving to break this technological barrier and has finally succeeded in the development of a new process technology based on a totally new concept called MPS technology. This technology achieves low-k film boasting a desired dielectric constant lower than 2.5 without sacrificing compatibility to various requirements for the 45nm-node interconnect module. With this technology, silica molecules with silicon and oxygen atoms, which are designed as a circular chain enveloping a pore, are piled up on the silicon wafer in a vacuum chamber. By designing the silica-based molecule structure to contain a pore of a desired size in advance, the pore size and the volume fraction in the product porous low-k film can be intentionally controlled. In our research, a precursor silica molecule containing a pore smaller than 1nm was prepared. Using this precursor, MPS low-k film with a dielectric constant of 2.4 was successfully formed by a plasma-activated deposition process.

As a result of this achievement, by combining this novel MPS low-k film with advanced transistors, which are currently being developed for 45nm-node LSIs, a 50% reduction in chip area and a 20% cut in power consumption as compared to 65nm-node LSIs will be realized for a similar level of circuit volume. The introduction of 45nm-node LSI devices into next-generation high-speed network severs and multi-functional, mobile terminals is expected to contribute significantly to the establishment of environmentally-friendly IT infrastructure.

NEC, NEC Electronics, and MIRAI Project, believing that copper interconnect module technology based on MPS porous low-k film is essential to realizing 45nm-node, low power LSIs, are working toward the early realization of its introduction into the market place.

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Notes:
Molecular-pore-stacking technology: This is a new-concept low-k deposition process, in which silica-based precursor molecules, whose molecular structure is designed to contain a circular chain enveloping a pore, are piled up on the silicon wafer in a vacuum deposition chamber. In contrast, for conventional porous low-k films formed by the chemical deposition method, introduction of the porous structure into the film takes place during the event of chemical binding of precursor molecules. The MPS approach is more advantageous in achieving regularity of pore sizes and spacing, whereas the conventional approach may suffer from unwanted pore-aggregation, which degrades the macroscopic robustness such as mechanical strength as a higher porosity is pursued to obtain lower k.

Pore seal structure: This is an interconnect structure, in which the etched side-wall of the line trench and the vias in MPS low-k film are covered with ultra-thin, dielectric liner film. By using NEC's original plasma-polymerization film, the pore-seal-structured interconnects reveal excellent insulation endurance in the narrow-spaced lines. The pore seal film has Cu diffusion barrier property, improving insulation reliability under high electrical stress.

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