ARM Artisan Low Power IP Offered By IBM, Chartered To Support 65-nm Common Platform

June 6 2005

ARM today announced a collaboration with IBM and Chartered Semiconductor Manufacturing that makes available the ARM Artisan Metro low-power platform for the IBM-Chartered 65-nanometer low-power common process platform. The 65nm agreement leverages the companiesâ€™ collaborative development efforts for the IBM-Chartered 90nm common platform and validates their continued commitment to be at the forefront of providing leading-edge design and manufacturing solutions.

"Collaboration on process technology, IP and design methodologies are central themes in IBMâ€™s strategy and key to driving the economics of the semiconductor industry," said Steve Longoria, vice president, Semiconductor Technology Platform for IBM. "The IBM-Chartered cooperation with ARM in the development and deployment of physical IP with sophisticated power management capability for our 65nm platform is yet another example of the execution of this strategy."

"Through strategic collaboration with leading companies in the design community, such as ARM, the common platform is increasingly recognized by semiconductor companies as a lower risk and more cost-effective business model to access advanced process and design technologies," said Kevin Meyer, vice president of worldwide marketing at Chartered. "Optimizing these technologies for world-class manufacturing with an open IP model that facilitates true multi-sourcing

is a distinctive and compelling customer benefit of the IBM-Chartered common platform."

The newly available ARM IP products include the Artisan Metro low-power standard cells, I/Os and memories that are optimized for low-power designs. The physical IP products incorporate the combined expertise of IBM, Chartered and ARM in addressing the complexities of power management and design for manufacturability with the industryâ€™s first third-party, low-power IP available today for a foundry 65nm process.

All ARM physical IP products are characterized for timing and power over an extended range of voltages, enabling designers to perform accurate pre-tape out simulation of multi-voltage designs. The IP conforms to the Artisan design standard supporting recent releases of leading EDA tools that simplify power-optimized design and increase design productivity. The suite of products enables advanced power management methodologies by providing library components such as voltage level shifters and power gating cells for use with both memories and standard cell blocks.

"Solving technical problems across company boundaries and offering choices to customers is what fuelled the growth of the foundry model," said Neal Carney, vice president of Marketing, Physical IP, ARM. "This collaboration with Chartered and IBM sends a message to the industry that the economics of the common platform model are alive and well at 65nm."

Citation: ARM Artisan Low Power IP Offered By IBM, Chartered To Support 65-nm Common Platform (2005, June 6) retrieved 19 April 2024 from https://phys.org/news/2005-06-arm-artisan-power-ip-ibm.html

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.