Cadence and Faraday Announce Library Collaboration for Nanometer Design

May 9 2005

Cadence Design Systems, Inc. and Faraday Technology Corporation today announced that Faraday has joined the OpenChoice intellectual property (IP) program to co-develop with Cadence an extensive list of library views. The libraries are being designed to facilitate digital implementation and signal integrity (SI) under UMC's 130-nanometer Fusion process.

The library view generation process will be qualified and validated by both Faraday and Cadence research and development teams. Under the process, Faraday's customers will have the ability to handle digital implementation and SI signoff in the Cadence Encounter digital IC design platform.

"As a long-term partner of Cadence and library provider for UMC, we are very excited with this collaboration because it allows Faraday to handle signal integrity issues for our common clients at 130 nanometers and below. We are very pleased with this extended relationship with Cadence because we were able to qualify and validate all our co-developed library views through Cadence's OpenChoice IP program," said Jim Wang, Director of Design Development at Faraday Technology.

"To facilitate a smooth path to silicon success for our customers, Cadence is committed to open programs and standards like OpenChoice and the effective current source model (ECSM)," according to Jan Willis, senior vice president, Industry Alliances at Cadence. "We're delighted to work with Faraday to leverage our open approach and

technology to provide customers with a new, SI-aware path to silicon."

Ken Liou, director of UMC's IP Development and Design Support Division, said "Faraday's collaboration with Cadence to address SI issues at the IP level helps customers achieve faster, first-pass silicon success. We are pleased that Faraday's standard cell libraries have been validated on our 130-nanometer Fusion process."

The co-development between Cadence and Faraday has spawned a list of library views for the UMC 130-nanometer Fusion process, high-voltage threshold (HVT) and low-voltage threshold (LVT) mixed library, including both standard logic cells and input/output (I/O) cells. The library views include qualified layout exchange format (LEF), required by chip implementation in SoC Encounter, which features routing by NanoRoute; power grid views (PGV) for VoltageStorm® power rail analysis; and noise library (cdB) and ECSM for CeltIC NDC SI-aware delay calculation and crosstalk glitch analysis. Libraries for other processes will be available from Faraday soon.

Citation: Cadence and Faraday Announce Library Collaboration for Nanometer Design (2005, May 9) retrieved 26 April 2024 from https://phys.org/news/2005-05-cadence-faraday-library-collaboration-nanometer.html