

STMicroelectronics Manufactures 90nm Silicon of World's First Multi-Standard Disk-Drive Physical-Layer IP

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STMicroelectronics (NYSE: STM) today revealed successful fabrication of the MIPHY (Multi-Interface PHY) Physical Layer interface IP (Intellectual Property) using 90nm technology. This macro-cell, the first to support Serial ATA (SATA) disk drives, as well as applications using the Serial Attached SCSI (SAS), Fibre Channel, and PCI Express serial interface standards has been designed by ST's engineers to be integrated with other functions into a System-on-Chip (SoC) and allow drive manufacturers to reduce costs by building and stocking one IC to operate in multiple drives.

By implementing and verifying the 90nm interface design now, ST is preparing for the migration of SoC products to 90nm technology later this year, benefiting from the lower power requirement and smaller physical size. Proven IP will be ready ahead of time to minimize the time-to-market for new products and reduce the development costs of new ASICs. In addition, the multiple-standard capability of the new macro-cell will enable fast design validation for different markets and will eventually yield the benefit of larger scale volume production while at the same time reduce costs for manufacturers by optimizing their engineering resources.

Exceptional performance results have been seen in preliminary evaluation of the first silicon of this new interface, with a total jitter (deterministic and random) measured at less than 50ps (picoseconds).

Such performance has been achieved by the use of a new Time-Base Generator that integrates a harmonic PLL (Phase Locked Loop) to minimize random jitter - less than 2 ps – and provides high noise rejection in every working environment.

The MIPHY IP extends the capability of ST's existing SATA310 'hard macro', which is currently integrated into hard disk drive controller ASICs, manufactured in ST's 0.13-micron technology. SATA310 meets all the requirements of the SATA specification and has been tested successfully with all available SATA-compliant products from other vendors. ST has developed the new IP working closely with strategic customers and addressing their specific requirements. The Company is planning to integrate the MIPHY in its next-generation 90nm SoC scheduled to tape-out in the second half of 2005.

These Physical Layer macro-cells perform the high-speed serialization and de-serialization function and provide a 20-bit wide parallel interface to the link layer. In Serial ATA applications they can perform either host or device operations, and can drive external signals directly without needing additional external components.

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