SEMATECH Identifies Top Technical Challenges for 2006; Adds Transistor Scaling

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SEMATECH today announced its Top Technical Challenges for 2006, continuing to underscore advanced gate stack, 193 nm immersion and EUV lithography, mask infrastructure, and low-k dielectrics with process compatibility. Consortium leaders also placed planar bulk transistor scaling on the list for the first time.

SEMATECH uses the Top Challenges to focus its resources on the most critical of approximately 75 projects that it maintains in key areas of semiconductor and related R&D. The SEMATECH research portfolio is developed by the consortium's Executive Steering Council (ESC), in consultation with corporate managers.

“SEMATECH continues to remain at the forefront of semiconductor R&D, and this set of challenges reflects our commitment to that goal,” said Michael R. Polcari, SEMATECH president and CEO. “This list also reflects the guidance of our member companies on how to best use our skills and resources to benefit SEMATECH's members and the industry. We'll address many of these issues in collaboration with our R&D partners, including the university researchers investigating promising semiconductor technologies in our Texas-based Advanced Materials Research Center.” (www.amrctx.org)

The SEMATECH challenges reflect the consensus of the consortium's member companies, and are grouped below by technical area:

Lithography

-- **Immersion Lithography** has been developed as a method for extending the resolution and depth of focus of optical lithography, by interposing a liquid between an exposure tool's projection lens and a wafer. Prototype immersion tools are beginning to arrive in advanced manufacturing fabs. SEMATECH's focus is on resolving the few remaining manufacturability issues, such as coating durability. An additional program will determine the extensibility of 193 nm immersion to 45 nm half-pitch and beyond.

-- **Mask Infrastructure** is critical to improving the capabilities and reducing the overall cost of photomasks for both 193 nm immersion and extreme ultraviolet (EUV) lithography. SEMATECH's programs are focused on developing the tools and technology to ensure the evolution of cost-effective mask solutions for future lithography generations.

-- **Resist Strategy** includes determining the practical and theoretical limits of chemically amplified resist platforms on developing new materials approaches for 193 nm immersion; and emphasizing ultimate resolution, line edge roughness (LER) and sensitivity for EUV resists. SEMATECH recently sponsored workshops in resist limitations and line edge roughness as part of the 2005 SEMATECH Knowledge Series, a collection of single-focus industry meetings designed to increase global knowledge in key areas of semiconductor R&D.

-- **EUV Infrastructure** includes the development of critical technology components to enable the introduction of extreme ultraviolet lithography into manufacturing later in the decade. SEMATECH will continue to focus on assessing the status and developing solutions for defect free mask blanks, EUV sources, optics lifetime, mask handling and photoresists.

Front End Processes

-- **Advanced Gate Stack**, involving development of high-k dielectrics for logic and memory products, metal gate electrodes, dual workfunction metal gate transistor processes, and various electrical characterization methods for metal/high-k devices. The Advanced Gate Stack (AGS) Program focuses on delivering reliable gate stack technology for the 45 nm node and beyond. To support this effort on an industry-wide basis, SEMATECH's AGS Program will host its Second International Workshop on Advanced Gate Stack Technology, Sept. 26-27 at the Omni Hotel in downtown Austin.

-- **Non-classical CMOS**, an approach to the challenges posed by increasingly microscopic scaling of chip features. Non-classical CMOS includes infrastructure development for alternative device technologies, such as strained silicon, silicon-on-insulator (SOI) double-gate metal-oxide semiconductor field-effect transistors (MOSFETs) and multi-gate FETs (MuGFETs).

-- **Planar Bulk Transistor Scaling**, which will cover the development of technologies to enable the continuation of conventional MOSFET scaling for as long as possible. Potential solutions include channel material engineering (GeOI, III-V channel, hybrid silicon); advanced strain engineering; new doping and annealing approaches; and metallic junctions. SEMATECH's AMRC university partners will contribute significantly to this work.

Interconnect

-- **Low-k Dielectrics and Process Compatibility –** Low-k is critical to advanced semiconductor manufacturing because it reduces line-line capacitive coupling and allows metal lines to be packed closer together

on a chip, with less risk of electrical signal leakage. After identifying and screening a number of new low-k materials, SEMATECH engineers are evaluating two low-k candidates in two-level metal integration work that have the potential to advance k-effective to 2.5 for the 45 nm technology node. Additionally, SEMATECH technologists will work to understand and address the resistivity rise in narrow copper lines, and the development of advanced barrier and fill solutions.

Manufacturing

-- **Metrology**, a critical enabler to the achievement of increasing device densities and decreasing feature sizes on advanced semiconductors. Metrologists at SEMATECH will e valuate commercially available metrology tools for critical dimension scanning electron microscopy (CD-SEM), optical critical dimension (OCD) and overlay, and commercial defect inspection and redetection tools, for the 45 nm technology node and beyond. This work will free SEMATECH member companies from having to do such benchmarking on their own.

-- **Manufacturing Effectiveness and Productivity**, a series of factory- and equipment-related projects aimed at improving both equipment and overall factory productivity, and reducing costs in today's and tomorrow's fabs. These projects include e-manufacturing; advanced equipment and process control; advanced equipment software testing; short cycle time and short ramp-ups; equipment and fab agility; and standards development. Progress in these areas will be featured at the ISMI Symposium on Manufacturing Effectiveness (sponsored by the International SEMATECH Manufacturing Initiative) Oct. 24-26 in Austin.

Environment, Safety and Health

-- As a cross-cut priority for each of the Top Challenges, ESH addresses issues emerging from the introduction of new materials and process chemicals into advanced manufacturing. SEMATECH ESH engineers are focusing on timely assessments of the potential impacts of new materials and processes; industry response to growth of environmental regulations; ergonomic issues arising from tool complexity and larger wafer sizes; and resource conservation, especially in the area of tool energy consumption.

“SEMATECH remains committed to finding cost-effective and manufacturable solutions to all of these challenges,” said Polcari. “In doing so, we will continue to deliver value to our members while accelerating the next technology revolution for the semiconductor industry.”