Freescale, Soitec achieve 70-percent improvement in electron mobility using strained SOI technology for sub-65-nm device

April 12 2005

Marking an important advancement in strained silicon technology for next-generation devices, Freescale Semiconductor, Inc. and the Soitec Group today announced the results of their joint development effort to optimize CMOS device performance at the sub-65-nm nodes using strained silicon-on-insulator (sSOI) engineered substrates. With device results revealing an approximate 70-percent increase in electron mobility, as well as high compatibility with existing SOI CMOS processes, the collaborative effort demonstrated that 45-nm CMOS devices built using strained SOI substrates can effectively take device performance to the next level - ultimately enabling Freescale to bring faster, more power-efficient next-generation chips to market.

Company officials report that they launched the collaborative effort two years ago to evaluate strained SOI as the potential base material for sub-65-nm devices and beyond. By combining Soitec's Smart Cut™ technology and engineered substrate expertise with Freescale's advanced CMOS process capabilities, the development team was able to produce the industry's first functional 45-nm CMOS devices on bonded strained SOI substrates.

To satisfy CMOS integration requirements for tomorrow's high performing chips, Soitec and Freescale worked in close cooperation to optimize the critical relationship between the transistor architecture and

the strained SOI substrate. “Substrate quality and uniformity are critical to ensuring the best possible device performance. Together, the two companies were able to leapfrog existing processes – pushing the material to accommodate partially depleted devices, as well as enable rapid improvement in transistor performance,” said Joe Mogab, senior technical fellow and director of the Advanced Products Research and Development Laboratory for Freescale Semiconductor. “This strategic research partnership with Soitec has allowed us to tap into a wealth of expertise to accelerate evaluation of these materials.”

“We are extremely pleased with the results already being achieved through our technical collaboration with Freescale,” said Carlos Mazuré, Soitec’s chief technical officer. “This alliance is an excellent example of the strong synergy chipmakers and substrate suppliers can create to both accelerate the substrate engineering process and specifically tailor it to achieve the desired device performance.”

Optimizing Technology Applications & Outcomes:

The initial work performed was based on silicon germanium-on-insulator, followed by sSOI, allowing both Soitec and Freescale to learn how to match a strained SOI substrate with a device design to optimize the technology applications and outcome. sSOI is a strong candidate for the sub-65-nm technology nodes due to its unique ability to address high-performance, low-power-consumption applications.

NMOS device results on strained SOI exhibited a mobility increase of approximately 70 percent. Electrical reliability data showed no difference between standard SOI and sSOI devices. Furthermore, no relaxation of the strained silicon was observed at 40-nm transistor geometries. The ability to produce strained silicon with thicknesses above 40 nm makes sSOI highly compatible with existing SOI CMOS processes.

SOI material, which incorporates a layer of silicon on an embedded layer of silicon dioxide, enables chips built on the substrate to function at significantly higher speeds with less electrical loss—enabling a two to three times reduction in power consumption, and a 20- to 30-percent improvement in device speed. Similarly, strained silicon allows electrons to experience less resistance and flow faster, resulting in a 20- to 30-percent increase in transistor performance. Combining these technologies, in the form of strained SOI material, will enable Freescale to realize the cumulative benefits of both technologies, permitting significant advances in device speed, power consumption and IC packing density.