# Freescale, Philips and STMicroelectronics Expand Industry's Largest R&D Alliance

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The Crolles2 Alliance partners STMicroelectronics, Philips and Freescale Semiconductor have reached a preliminary agreement to cooperate on the creation and validation of high-level System-on-Chip (SoC) intellectual property (IP) blocks. Implementation and completion of this agreement is still subject to the successful conclusion of a contract between the partners.

The companies already work together as part of the Crolles2 Alliance in the research, development and industrialization of CMOS process technologies. The Alliance partners see a bundling of effort in generation, validation and support of high-level SoC IP blocks as a logical next step. The goal is to shorten the time-to-market for the increasingly complex chips demanded by today's systems.

The three Alliance partners plan to set up the Library and IP Partnership (LIPP) with operations across a number of sites. Potential sites include Grenoble, France, Eindhoven, The Netherlands, Austin, Texas and Bangalore and Noida in India, with headquarters in Eindhoven. LIPP will provide and support high-value re-usable SoC IP blocks that the partners will use in their System-on-Chip (SoC) designs at the 65nm CMOS node and beyond. Shared development of these standard yet design-intensive IP blocks means that each of the Crolles2 Alliance partners will be free to concentrate on its individual system-level competencies in the delivery of advanced SoCs to its customers. Consumers will benefit from earlier introduction of even more advanced multimedia and communications features in products that utilize the

Crolles2 Alliance partners' SoC solutions.

The three partner companies already share a common set of design rules and foundation library sets as part of the Crolles2 Alliance joint technology development activities. The preliminary understanding is to extend this alignment to include their SoC IP blocks and re-use methodology.

"The preliminary understanding represents a major step forward in overcoming the design gap – one of the biggest challenges for the semiconductor industry," said Bart De Loore, newly appointed general manager of the Alliance LIPP and former general manager of Philips Semiconductors IP ReUse Technology Group. "It is the first time in the industry that a group of major semiconductor companies has agreed to share proprietary SoC IP blocks. This move is designed to help the Alliance partners roll out complex right-first-time SoCs faster than ever before from their advanced CMOS process technologies."

Staff for the new Alliance LIPP organization initially will be drawn from the Alliance partners. Some of the first projects undertaken will be the development of re-usable IP blocks for advanced I/O interface standards, common analog IP blocks, embedded processors and SoC infrastructure IP for the Alliance's 65-nm CMOS process.

In the context of SoC architectures and IP re-use, LIPP will also coordinate the participation of Alliance partners in industry standardization initiatives such as Structure for Packaging, Integrating and Re-using IP within Tool-flows (SPIRIT), Open SystemC Initiative (OSCI), and Virtual Socket Interface Alliance (VSIA).