Engineers Achieve Breakthroughs Enabling Implementation of High-k Dielectrics at 45 nm Technology Node

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Using a selected set of tools and processes, Sematech engineers have achieved twin breakthroughs in channel mobility and reliability of high-k/metal gate transistors, putting high-k technology for CMOS within reach at the 45 nm technology node.
The Sematech advance involves a titanium nitride (TiN) metal gate on a hafnium silicate (HfSiO) dielectric with an equivalent oxide thickness (EOT) of roughly 10 angstroms (Å), with mobility at 90 percent of the universal mobility curve for silicon dioxide (SiO_2), the historic gate dielectric material. These EOT and mobility metrics meet the 45 nm technology node specifications listed by the International Technology Roadmap for Semiconductors (ITRS).

The achievement caps a lengthy effort within Sematech's Front End Processes Division, and is part of a program to fully enable the eventual introduction of high-k/metal gate technology in volume manufacturing. The process is not expected to add significant cost to current CMOS product flows.

“SEMATECH's high-k process represents a significant step in the search for a complete solution to planar CMOS at the 45 nm node and beyond,” said Byoung Hun Lee, manager of the Advanced Gate Stack Program. “We are also working to produce a dual metal gate that can work with this process. Plus, these breakthroughs have applications for specialty architectures, such as FinFETs [an advanced type of field-effect

transistor] or fully depleted SOI [silicon on insulator] devices.”

Tests of SEMATECH wafers at Yale University confirmed the quality of the high-k dielectrics, according to T.P. Ma, chairman of Yale's Department of Electrical Engineering. “The mobility results that we recently obtained on SEMATECH's test wafers were truly outstanding, which are consistent with the low densities of interface traps in these wafers. Having seen these results first-hand, I am a lot more optimistic than ever before about the practical implementation of high-k gate dielectrics in the foreseeable future.”

In explaining the significance of the SEMATECH process, Lee said that new materials and techniques must be found for transistors as their size decrease into the deep sub-100 nm regime. One of the serious challenges the industry faces is developing new gate dielectric materials. For decades, silicon dioxide (SiO_2) was a reliable dielectric, but as transistors have continued to shrink, the reliability of the SiO_2-based gate dielectric is reaching its physical limits, while the technical challenges of using that dielectric are increasing rapidly.

One solution is to use other materials, such as hafnium-based metal oxides, for gate dielectrics. These high-k materials, so-called because of their high dielectric constant (k), can be made much thicker than SiO_2 while achieving the same gate capacitance - the ability to turn a gate on and off, allowing it to process data. SEMATECH has aggressively pursued the high-k option for the past eight years, in broad collaboration with several universities and equipment suppliers to identify materials and processes in time to meet member company and industry manufacturing needs.

Lee noted that in order to implement metal/high-k technology at the 45 nm node, slated by the ITRS for initial volume production in 2010, metal/high-k devices must perform well in three areas: mobility,

reliability, and threshold voltage (V_{th}) controllability.

Mobility is the speed at which an electron can travel through a material, such as silicon channel region. Critical to electron mobility in a silicon-based transistor is the interface between silicon and the gate dielectric, with the SiO_2 gate dielectric setting the standard. While high-k dielectrics historically have tended to show low electron mobility, SEMATECH's Hf-silicate performed at 90 percent of universal mobility, which is very close to a SiO_2-based gate dielectric at similar EOT.

Also, Lee said SEMATECH's Hf-silicate process demonstrated exceptional results not only for mobility, but also for reliability, as measured by V_{th} instability. For an optimized process, the SEMATECH material reached one of the project's goals by showing a V_{th} instability of less than 10 millivolts (mV) after 1,000 seconds of constant voltage stress at 22 megavolts per centimeter (MV/cm). This result is about 10 times better than the comparable reliability of high-k materials typically shown in industry reports.

“What this means is that we have a high-k process with mobility similar to the heavily nitrided silicon oxynitride [SiON] dielectric which is currently in manufacturing, but with reduced gate leakage current,” said Paul Kirsch, manager of SEMATECH's Advanced Gate Dielectric Project. “We have established a tool set and have identified several process parameters to reach this point.” Kirsch added SEMATECH is making rapid progress in solving the challenge of V_{th} controllability and plans a subsequent announcement on that issue.

“This is a significant enabler for SEMATECH member companies to continue traditional planar CMOS transistor scaling,” Lee said. “As manufacturers make their decisions on how to approach the 45 nm node, they will find that SEMATECH's work enhances the availability of high-k for that node. Our expectation is that within a year, we will resolve the

key issues in the implementation of metal/high-k gates stack into conventional CMOS flow."

Lee credited Kirsch and SEMATECH engineers Naim Moumen, Prashant Majhi, Seungchul Song, Rino Choi and Gennadi Bersuker with developing these breakthroughs in the consortium's high-k dielectric process.

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