TI Delivers Industry's First Wireless Digital Baseband Processor on Advanced 65-nm Process

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Texas Instruments Incorporated (TI) (NYSE: TXN) announced it is delivering fully functional wireless digital baseband devices from its advanced 65-nanometer (nm) CMOS process technology. The announcement fulfills TI's commitment made one year ago when it disclosed details of the 65-nm process and techniques to shrink the 90-nm design area by half, leverage strained-silicon to boost transistor performance by 40 percent, and reduce leakage power from idle transistors by a factor of 1000. TI is among the first semiconductor manufacturers to deliver working 65-nm products.

TI's 65-nm process technology gives us the ability to pack hundreds of millions of transistors that support both analog and digital functionality in tightly integrated system-on-a-chip (SoC) solutions," said Dr. Hans Stork, chief technology officer of Texas Instruments. "By delivering the industry's first 65-nm device for the wireless market, TI is giving mobile customers access to more processing performance for the most advanced applications in a smaller, lower power chip."

65-nm Innovations Will Extend Battery Life

With advanced multimedia and high-end digital consumer electronics functionality increasing processing demands, a focus on low power semiconductor technologies has become of heightened importance. To address this concern, TI has implemented several innovative power

management techniques in its 65-nm platform.

First is TI´s SmartReflexTM dynamic power management technology that automatically scales power supply voltage based on user performance demands and helps control power consumption in devices like TI´s OMAPVoxTM processors. By closely monitoring circuit speed, SmartReflex can dynamically adjust voltages to meet the exact performance requirements without sacrificing overall system performance. As a result, minimum power is used for each operating frequency, extending battery life and reducing the amount of heat produced by the device.

TI applies other techniques at 65-nm to reduce the power consumed by transistors when they are idle, including the time when a mobile phone is in standby mode waiting to receive a call. These innovations include back-biasing of SRAM memory blocks and retention flip-flop circuitry that allows voltages to drop extremely low without requiring a rewrite of logic or memory content. Together these advancements can deliver up to a 1000 times reduction in power leakage.

"Texas Instruments continues to execute on a manufacturing and technology development strategy that is second to none," commented Len Jelinek, principal analyst for iSuppli Corporation. "TI's advances in 65-nm manufacturing technology have raised the bar of excellence for companies designing CMOS technology for mobile wireless applications, consumer products and microprocessors."

SoC Design Flexibility

TI continues its approach of offering several optimized process recipes to balance the unique needs of end products or applications. This is done through adjustments to the transistors´ gate length, threshold voltage, gate dielectric thickness or bias conditions for example. The 65-nm

design library offers an unprecedented number of options for maximum design flexibility and optimization.

A very low power offering extends battery life in portable products such as 3G wireless handsets, digital cameras and audio players with increasingly sophisticated multimedia features. A mid-range offering supports DSP-based products and TI´s high performance ASIC library geared toward communication infrastructure products. The highest performance version of TI´s 65-nm process supports Sun Microsystems´ UltraSPARC® family of 64-bit processors.

Enabling Analog and Digital Integration

The 65-nm process will support TI´s revolutionary DRPTM architecture in future products to integrate digital RF functionality in single-chip wireless solutions. By processing RF functionality in digital CMOS, TI reduces the manufacturing cost and power consumption of the transmit and receive functions, and frees up much-needed board space for advanced applications and functionality.

Additionally, TI includes access to ASIC libraries that support a range of different threshold voltage transistors that can be combined to optimize circuitry for power consumption or high performance. This includes a number of analog/mixed signal macros that use optimized analog transistors and high-density MIM capacitors. For SoC designs, especially those targeted for portable systems where silicon area is premium, integrating analog functions can enable lighter-weight, less expensive, more mobile applications.

Leveraging Latest Materials and Manufacturing

The 65-nm process includes up to 11 layers of copper interconnect

integrated with a low k dielectric, OSG, with a k (dielectric constant) of 2.8 - 2.9. Low-k materials reduce active power consumption, as well as capacitance and propagation delays within the interconnect layers of a device, thereby boosting overall chip performance. Other improvements include an induced strain on the transistor channel during chip processing to increase electron and hole mobility; nickel silicide to lower both gate and source / drain resistance, and ultra-shallow source / drain junctions. A unique use of differential offset spacers allows independent optimization of the NMOS and PMOS transistors, driving performance and minimizing leakage.

TI's 65-nm process is planned for both 200mm and 300mm production, with fully qualified production expected in late 2005.