Silicon Design Chain Collaboration Demonstrates Significant 90-nanometer Total Power reduction

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Industry leaders, working through the Silicon Design Chain Initiative, today announced new, silicon-validated, low-power design techniques to achieve total power savings of over 40 percent on a 90-nanometer test design. The low-power design employed an ARM1136JF-S test chip, ARM Artisan standard cell libraries and memories, Cadence Encounter design platform and TSMC's Reference Flow 5.0. Applied Materials, Inc., ARM, Cadence Design Systems, and Taiwan Semiconductor Manufacturing Company (TSMC) form the Silicon Design Chain Initiative.

"This is the first time industry leaders have banded together to correlate real power savings into real silicon, which should dramatically increase the adoption rate for 90 nanometer technology," said Edward Wan, senior director of design service marketing at TSMC. "This project exemplifies the power of strategic collaboration to significantly differentiate our respective technology offerings."

Power Management Challenges

Although mobile system-on-chips (SoCs) represent the largest semiconductor volume driver, they have proven challenging with respect to balancing increased complexity and power consumption. Advanced process technologies (i.e., 0.13-micron and below) accommodate demand for a variety of sophisticated functionality on a single mobile

chip at a reasonable cost. Chip developers are realizing that power management - whether to extend battery life or to minimize heat dissipation - must balance power and performance.

"Customers expect performance and long battery life from portable products. Freescale's MXC architecture is a highly integrated IC implemented in an advanced CMOS process requiring innovative power minimization methods," said Christopher Chun, Advanced Power Management System Architect, Freescale Semiconductor. "Many power reduction techniques are being investigated, but most significantly increase IC costs through increased design times. For robust and practical power reduction techniques, it is critical that process developers, IC designers, and IP and tool providers collaborate to automate the methodologies."

"Power management is a key technology concern for ARM Partners, especially in the wireless market, and ARM has always worked closely with them to achieve high-performance, low-power devices especially in the mobile and home markets," said Noel Hurley, CPU Product Marketing manager at ARM. "Combining ARM's processor and its Artisan physical IP expertise with that of Cadence's software and TSMC's process proficiencies to streamline a complete design-through-production flow, we believe, can provide additional value to a broad range of our Partners."

Meeting the Low-Power Design Challenge through Open Collaboration

For mainstream designers, an effective low-power design strategy has been largely unavailable because it required a significant development effort between intellectual property (IP) vendors, EDA providers, manufacturing equipment suppliers and independent silicon foundries

across the semiconductor design chain. The Silicon Design Chain Initiative was established by Applied Materials, ARM, Artisan Components, now part of ARM, Cadence and TSMC to provide proven design flows to solve the industry's most challenging nanometer design issues. Drawing on each company's domain of expertise, the Silicon Design Chain has correlated models, design and analysis tools, and IP to silicon results, providing customers with a proven path from design to volume production.

"The challenges of today's nanometer electronics are such that no one company can address all of them alone," said Jan Willis, senior vice president, Industry Alliances at Cadence. "It takes the coordinated resources and expertise of numerous domain experts across the design chain to enable our customers to develop nanometer-scale products successfully. Cadence is pleased to collaborate with other leaders through the Silicon Design Chain to create innovative solutions that can provide growth opportunities for the entire industry."

In close collaboration, members of the Silicon Design Chain Initiative have developed an integrated power management methodology that optimizes SoC power and performance, with minimal disruption to existing RTL flows. This simplified approach combines design implementation tools such as Cadence Encounter digital IC design platform, Encounter RTL Compiler synthesis, Encounter CeltIC™ NDC (Nanometer Delay Calculator) signal integrity analysis and VoltageStorm® power analysis with the ARM's Artisan standard cell libraries and memories, including support for the Cadence effective current source model (ECSM) format through lib_ecsm library views for standard cells.

"Power consumption is one of the major issues facing our industry as we move to the 90-nanometer technology node and beyond," said Mike Smayling, chief technology officer of the Maydan Technology Center at

Applied Materials. "We are excited by the work done by our fellow members of the Silicon Design Chain in developing this important low-power design solution, and will continue to support these critical projects by providing the process and inspection technologies needed to enable these advanced chip designs."