Cadence Delivers Industry's First Full-chip Test Technology

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Cadence Design Systems, Inc. today announced Cadence Encounter Test Architect, the industry's first full-chip test architecture development product. It includes the industry's first unified compiler-based methodology for full-chip test. The result is faster development of a higher-quality test infrastructure than is currently possible with point test tools.
Based on a unique test infrastructure compiler, Encounter Test Architect supports a unified methodology for specifying, compiling, and verifying full-chip test. This includes scan, compression, memory BIST, on-product clock generation, boundary scan, and I/O test.

Currently, designs can contain a number of cores, hundreds of memories and a complex hierarchy of RTL blocks. To create the necessary full-chip test today, test teams separately specify, implement, and verify each structural element—typically with different tools—and manually create the test infrastructure that ties everything together. This tedious, time-consuming, error-prone process is increasingly responsible for silicon re-designs, unnecessarily high cost of test, and poorer product quality.

"Kawasaki Microelectronics (K-Micro) worked closely with Cadence as it developed key components of Encounter Test Architect," said Yoshihito Nishizaki, Group Chief, CAD System Front End, Kawasaki Microelectronics. "We achieved excellent results with Encounter Test's OPMISR+ compression and OPCG (On Product Clock Generation) for delay test, including True-Time delay test, on many of our designs. We believe that this unified compiler-based methodology is a highly

effective way to create high-quality yet low-cost test infrastructures for nanometer designs."

Encounter Test Architect's methodology is based on test infrastructure compilation. Test engineers use the product's unified environment to specify, compile and verify full-chip test capabilities, including the individual test structures and the hierarchical (or flat) test infrastructure.

The Encounter Test Architect infrastructure compiler includes a new robust memory BIST capability with high fault coverage, easy BIST engine sharing, and automatic insertion and connection across the design hierarchy. The Encounter Test Architect team worked closely with ARM® to develop and validate the memory BIST solution. This ensured product interoperability and Encounter Test Architect's support of all ARM-recommended test algorithms.

"As a leading semiconductor memory provider, ARM is committed to providing customers with solutions that enable the successful design of complex system-on-chips (SoCs)," said Neal Carney, vice president of marketing, ARM Physical IP. "We believe that our memory generators, when coupled with Encounter Test Architect, will help provide high-quality, cost-effective and efficient solutions to help designers reach silicon success."

Customers will benefit from Encounter Test Architect with increased productivity, accelerated time to tapeout, reduced cost of test, and improved end-product quality.

"Test teams have become bogged down in trying to piece together their test infrastructures using a set of inconsistent point tools," said Paul Estrada, general manager of Encounter Test at Cadence. "Encounter Test Architect's unique compiler-based methodology delivers superior internal test structures with automatic test infrastructure compilation and

verification—all from a single specification. This is a huge step forward for test teams working on complex SoCs designs."

Encounter Test Architect will be available for shipment at the end of April 2005.