

# STMicroelectronics Uncovers the Future of Digital Video Broadcast and RF Integration

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STMicroelectronics, one of the world's most innovative semiconductor companies, will present a record twelve papers at this year's International Solid-State Circuits Conference (ISSCC) in San Francisco, California, during February 6-10, 2005. ST's most notable contributions cover advances in Digital Video Broadcast and Radio Frequency (RF) integration in 3G applications. ST experts were also selected to chair the sessions on the latest developments in RF technologies.

"ST's strong presence at this prestigious conference will be extremely well perceived by our customers and their advanced development teams. Once again it confirms ST's leadership in those technologies used within its major applications, digital broadcasting and wireless communications," said Bob Krysiak, Marketing Director for the Home, Personal and Communications Product Groups at STMicroelectronics.

In the field of above-IC integration, ST researchers in partnership with the CEA (French Atomic Energy Commission) and CSEM (Swiss Center for Electronics and Microtechnology) laboratories will demonstrate the feasibility of a fully-integrated RF front-end for Wideband CDMA applications using above-IC Bulk Acoustic Wave filters. Designed and fabricated in a 0.25-micron BiCMOS technology that is enhanced with above-IC capabilities, this experimental chip is the first application of a filter on top of an IC. The above-IC approach dramatically reduces the number of external components and total board area in the mobile terminal, which results in shorter product development cycles and lower manufacturing costs.

The session on wireless receivers for consumer electronics has invited ST's research center in Crolles, France, to introduce a complete Digital Video Broadcast-T tuner, fabricated in a 120-nm CMOS technology on a single chip. ST's solution unveils novel approaches to overcoming CMOS intrinsic limitations (1/f noise, low supply voltage), including an original charge-pump design. This paper clearly points to a new trend in digital terrestrial and satellite TV tuners, where the complete System-on-Chip integration in standard CMOS minimizes the overall bill of materials.

In baseband processing, ST will report on two implementations of the second-generation satellite digital video broadcast (DVB-S2) codec. The added LDPC (Low-Density Parity Check) and BCH (Bose-Chaudhuri-Hocquenghem) codes enhance the error correction rates and approach the theoretical performance limit in the 130-nm CMOS version. The second test chip, built in low-leakage 90-nm CMOS, offers faster operation (300MHz) while using fewer blocks of custom high-speed memories. This kind of error correction coding holds a promising future for wireless LANs or any other high-speed digital communication in noisy environments.

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