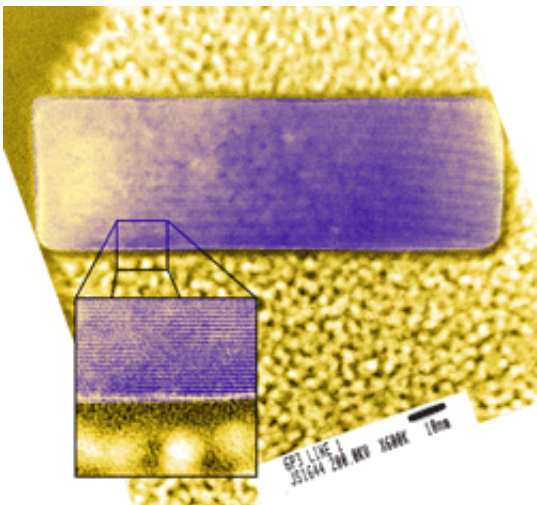


NIST Unveils Atom-based Standards

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Gaithersburg, MD--Device features on computer chips as small as 40 nanometers (nm) wide—less than one-thousandth the width of a human hair—can now be measured reliably thanks to new test structures developed by a team of physicists, engineers, and statisticians at the Commerce Department's National Institute of Standards and Technology (NIST), SEMATECH, and other collaborators. The test structures are replicated on reference materials that will allow better calibration of tools that monitor the manufacturing of microprocessors and similar integrated circuits.

The new test structures are the culmination of NIST's more than four-year effort to provide standard "rulers" for measuring the narrowest

linear features that can be controllably etched into a chip. The NIST rulers are precisely etched lines of crystalline silicon ranging in width from 40 nm to 275 nm. The spacing of atoms within the box-shaped silicon crystals is used like hash marks on a ruler to measure the dimensions of these test structures. Industry can use these reference materials to calibrate tools to reliably measure microprocessor-device gates, for example, which control the flow of electrical charges in chips.

"We have caught up to the semiconductor industry roadmap for linewidth reference-material dimensions with this work," says Richard Allen, one of the NIST researchers involved in the project. "With the semiconductor industry, one has to run at full speed just to keep up."

The new reference materials, configured as a 9 millimeter (mm) by 11 mm chip embedded in a silicon wafer, are now being evaluated by SEMATECH member companies. Compared to a batch of prototype test structures produced by NIST in 2001, the new reference materials offer a wider range of reference feature sizes, including some that are much narrower, and they are measured much more precisely (with uncertainties of less than 2 nm compared to 14 nm previously). In the absence of reference materials such as these, companies have calibrated measurement tools using in-house standards, which may neither be accurate nor agree with each other.

The new materials will be publicly unveiled at a workshop cosponsored by NIST and SEMATECH on March 2, in conjunction with an SPIE (International Society for Optical Engineering) meeting in San Jose, California. SEMATECH member companies have been invited to present the results of their evaluations of the prototype test structures at this meeting. The test structures could be distributed as NIST-traceable artifacts to end users in the semiconductor industry for development of metrology tools, or a private company could manufacture and distribute test structures based on the NIST technology.

The new silicon reference materials are the outcome of a series of technical and procedural innovations. First, rows of rectangular features are etched into a particular type of silicon wafer in which atoms are arranged in a regular lattice design. The features are about 150 nm high, arrayed in sets of six features, each with a different width. The lattice has extremely even edges, but NIST modified the etching process to make the sides of the features even smoother, which helped to improve measurement precision.

Using four different types of microscopes—optical, scanning electron (SEM), atomic force (AFM), and high-resolution scanning transmission microscopes (HRTEM)—the silicon reference features are first screened to identify those with the approximate right dimensions, and then very carefully measured. A key step in the calibration process involves passing a beam of electrons through the silicon lines to a detector. Alternating dark and light parallel lines on the detector mark where columns of silicon atoms diffract the electrons. Technicians then manually counted these marks. From this count, the dimension of the reference feature can be calculated, because the number of lines in the image matches the number of silicon atoms in the crystal, whose spacing is always exactly the same and is traceable to the international standard of length. These data can then be used to calibrate measurements by other microscope tools.

The program was a collaboration between NIST, SEMATECH, VLSI Standards Inc., San Jose, Calif. and Accurel Systems International Corp., Sunnyvale, Calif. NIST researchers handled the layout, etching, AFM imaging, and lattice plane counting tasks; a key step in the patterning of the silicon lines in the test structures was performed by VLSI Standards; the SEM imaging was performed by SEMATECH and NIST; and the HRTEM imaging was performed by Accurel Systems.

As a non-regulatory agency of the U.S. Department of Commerce's

Technology Administration, NIST develops and promotes measurement, standards and technology to enhance productivity, facilitate trade and improve the quality of life.

The members of SEMATECH cooperatively set global industry direction and accelerate technology solutions in infrastructure, lithography, materials, and manufacturing to ensure a strong and vibrant semiconductor industry.

Source: NIST

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