Infineon Developed Innovative Mixed-Signal Circuits That Redefine Power Limits in Standard CMOS

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At the IEEE International Solid State Circuits Conference 2005 in San Francisco (February 6 – 10, 2005) Infineon Technologies AG held several technical lectures presenting trend-setting results from its research laboratories. Two presentations were held in which two innovative circuit developments from the Development Center in Villach, Austria, were introduced. These research results describe high-performance D/A and A/D converters for demanding wireline and wireless communication tasks for the next generation of high-bandwidth products.

“The presentations held at ISSCC 2005 again underscore Infineon’s position as a technological leader in the continued development of crucial components for the communication solutions of the future,” said Manfred Haas, Head of the Infineon Development Center, Villach. “The new circuit concepts stretch the previous performance limits for standard CMOS components and enable us to use proven, economical processes to manufacture high-speed, power-saving chips. These innovative circuit concepts also satisfy the requirements that future generations of products for communication applications will have to meet in terms of power consumption and the capacity to handle a major increase in data volume.”

An extremely high-performance 12bit D/A converter has been specially developed for next-generation VDSL (Very High Data Rate Digital

Subscriber Line) systems. VDSL requires a very high resolution (12bits) combined with a high analog bandwidth (over 30MHz, for example). Infineon has developed a completely integrated, broadband delta sigma D/A converter for this. A new type of circuit architecture (time-interleaved double-data weighted averaging) makes efficient implementation possible in economical 130-nm standard-CMOS technology with a 1.5-V supply voltage. Power consumption is only 45mW, which means that it is about 50 percent less than is the case with conventional DA converters.

Oversampling and spectral shaping of the noise power make it possible to reach a high resolution of 12bits with the new D/A converter, at a corresponding signal frequency range of 30MHz. Furthermore, it was possible to keep the oversampling at a very low factor (an oversampling rate of 6), which provided the basis for a drastic reduction in power consumption. Modern CMOS technologies feature very low supply voltages, but this lowers the achievable signal amplitude and presents a considerable challenge for the development of D/A converters of this type. The Infineon solution is based on an optimized circuit technique that maximizes signal amplitude despite the low supply voltage. This makes it possible to process broadband signals (30MHz) at a high degree of linearity (76dB).

For mobile communications applications Infineon introduced an extremely efficient delta sigma A/D converter in 130nm CMOS technology. Besides a high degree of oversampling, the available noise power is also spectrally shaped. This makes it possible to achieve a high resolution of 74dB (12.5bits) with a corresponding signal bandwidth of 2MHz. The high-resolution A/D converter targets applications that are employed in the receivers used in cellular communications devices. Efforts are currently being undertaken to use digital circuits (such as channel filters or preamplifiers) to replace as many of the function blocks as possible that until now have been handled with analog

technology. This is raising the quality requirements for the AD converter, but dissipation power is to be reduced at the same time.

In recent years, the required performance improvements have essentially been gained by implementing new, faster process technologies. Now, however, the Infineon researchers have employed a new type of circuit architecture on the basis of a standard CMOS process to achieve a clear performance gain coupled with a reduction of dissipation power. The AD converter's dissipation power is 3mW with a 1.5V supply and a clock frequency of 104MHz. This made it possible to reduce power consumption for these innovative circuits down to 20 percent of the levels required by conventional A/D converters (4bit flash ADC). Through the development of special power-saving quantizers based on this new AD converter, talk times for cell phones can now be extended.